【Grant-in-Aid for Scientific Research (S)】

Broad Section J

Title of Project : Innovative Self-Learnable Architecture Platform for Accelerating Intelligent Computing

Masato Motomura
(Hokkaido University, Graduate School of Information Science and Technology, Professor)

Research Project Number : 18H05288 Researcher Number : 90574286
Keyword : Deep Neural Networks, Neuromorphic, Analog and in-Memory Circuits

【Purpose and Background of the Research】

With the advent of deep neural networks (DNNs), AI (Artificial Intelligence) technologies and societal applications are progressing rapidly. To make AI smarter and more energy efficient for realizing future "intelligent computing," not only software but also hardware (HW) technology is essential. To this end, this project brings together newest findings and research progresses in both DNN domain and neuromorphic HW domain, that aims toward more brain-like information processing, for creating an innovative architecture platform for accelerating future intelligent computing.

【Research Methods】

This project will be conducted by Integrated Architecture Research Laboratory and Integrated Nano-Systems Research Laboratory both at the same division of Hokkaido University. The former lab., led by the project leader, has presented binary DNN and log-quantized DNN accelerator HWs and the associated DNN learning methods, that have gained world-wide interests (Fig. 1).

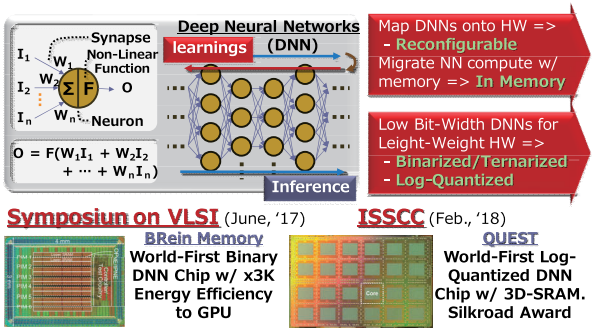

Figure 1. DNN Accelerators.

The latter lab., led by a sub-leader, professor Tetsuya Asai, has been working on analog-circuit oriented neuromorphic HWs (Fig. 2), and reserver computing that is gaining wide interests recently as a new wave in neuromorphic systems. The tight collaboration of these two labs working on related but different subjects is a key differentiation of the research formation at Hokkaido University.

Based on these on-going research activities, this project will try to establish 1) New circuit technologies for reconfigurable HWs for DNNs, 2)

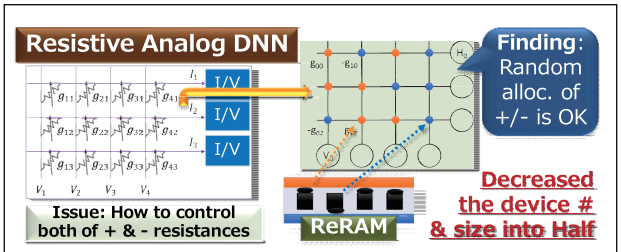

Figure 2. Neuromorphic HW technology.

inter-DNN-Neuromorphic learning systems and the associated HW architectures, 3) algorithm to circuits collaboration on creating high-energy efficiency HWs (including analog and/or in-memory circuit technologies).

【Expected Research Achievements and Scientific Significance】

The project will walk through whole the research chain from algorithmic researches to real HW developments and evaluations. As a final goal, we will try to establish self-learnable reconfigurable HW platforms, on-top of DNN and neuromorphic HWs, for future intelligent computing.

【Publications Relevant to the Project】

- Ando K., et.al., "BRein memory: a 13-layer 4.2 K neuron/0.8M synapse binary/ternary reconfigurable in-memory deep neural network accelerator in 65 nm CMOS," 2017 Symposium on VLSI Circuits [VLSI]. (Jun. 5-8, 2017).
- Ueyoshi K., et.al., "QUEST: a 7.49-TOPS multi-purpose log-quantized DNN inference engine stacked on 96MB 3D SRAM using inductive-coupling technology in 40nm CMOS," IEEE International Solid-State Circuits Conference [ISSCC] (Feb. 12-14, 2018).

【Term of Project】 FY2018-2022

【Budget Allocation】 148,300 Thousand Yen

【Homepage Address and Other Contact Information】

http://lalsie.ist.hokudai.ac.jp/en/