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研究課題名（和文）Thermal stability improvement of diamond logic circuits for high-temperature application

研究課題名（英文）Thermal stability improvement of diamond logic circuits for high-temperature application

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研究成果の概要（和文）：ワイドバンドギャップ半導体ダイヤモンドは、高温、高出力、高周波の電子デバイスの作製に適していることはよく知られている。最近、水素終端ダイヤモンドベース金属-酸化膜-半導体電界効果トランジスタ（MOSFET）論理回路などの作製は成功しましたが、アニーリング温度が300℃を超えるとうまく動作しません。本研究では、水素終端ダイヤモンドのオーム接触とMOSFETの熱安定性を改善するの目的であり、パラジウム/水素終端ダイヤモンドの比接触抵抗が低く、熱安定性が良いと結論が出る。 500度でアニールした後の二酸化ケイ素/水素終端ダイヤモンドMOSFEは安定に動作することができる。

研究成果の学術的意義や社会的意義
Thermal stability of hydrogen-terminated diamond MOSFETs are improved greatly. They can operate well at annealing temperatures as high as 500 ℃ for as long as one hour. This study is meaningful to the development of diamond MOSFETs and MOSFET logic circuits for high-temperature applications.

研究成果の概要（英文）：It is well-known that wide bandgap semiconductor diamond is suitable for fabrication of high-temperature, high-power, and high-frequency electronic devices. Recently, the hydrogen-terminated diamond (H-diamond) metal-oxide-semiconductor field-effect transistor (MOSFET) logic circuits such as are fabricated successfully. However, they cannot operate well as the annealing temperature higher than 300 ℃. Here, thermal stabilities for H-diamond Ohmic contacts and MOSFETs have been improved. A low specific contact resistivity and good thermal stability for the Pd/H-diamond are achieved. Good operations for the H-diamond MOSFETs after annealing at 500 degreeC are completed. Stable electrical characteristics are confirmed for the annealed H-diamond MOSFETs after 35 cycles repeat measurements. This study is meaningful to the development of H-diamond MOSFETs for high-temperature applications.

研究分野：電子デバイス・電子機器

キーワード：ダイヤモンド　トランジスタ　MOSFET

様　式　Ｃ－１９、Ｆ－１９－１、Ｚ－１９（共通）

１．研究開始当初の背景

(1) It is well-known that wide bandgap semiconductor diamond is suitable to replace silicon partly for fabrication of high-temperature, high-power, and high-frequency electronic devices [1]. In our previous studies [2-4], the hydrogen-terminated (H-diamond) metal-oxide-semiconductor field-effect transistors (MOSFETs) were fabricated with bilayer gate oxides deposited by atomic layer deposition (ALD) and sputtering deposition (SD) techniques. It was demonstrated that the SD-oxide/ALD-oxide/H-diamond MOSFETs showed good operations and enhancement-mode characteristics. Development of it provides a possibility to fabricate diamond electronic devices at low power consumption.

(2) Recently, the H-diamond MOSFET logic circuits such as NOT and NOR are fabricated successfully [5-7]. Their thermal stabilities have been investigated. There are distinct logical characteristics for the as-fabricated and 300 ºC annealed H-diamond MOSFET logic circuits. However, for the 400 ºC annealed one, the logical properties are damaged. There are several reasons for the poor thermal stability of H-diamond MOSFET logic circuits, such as damage of Ohmic contact for metal/H-diamond, degradation of oxide insulators, and high requirements of device fabrication process at high-temperature.

２．研究の目的

(1) Thermal stability of Ohmic contact for the metal/H-diamond will be improved. Different metals with work functions larger than that of the H-diamond will be formed. Annealing effects on surface morphology and contact resistance of metal/H-diamond will be investigated. The best Ohmic contact metal on the H-diamond with good thermal stability will be completed.

(2) Thermal stability of the H-diamond MOSFETs will be improved. After finding the best Ohmic contact metal on the H-diamond, the thermal stability of the H-diamond MOS capacitors and MOSFETs will be improved.

３．研究の方法

(1) High-quality H-diamond epitaxial layer is grown on the diamond substrate by microwave plasma-enhanced chemical vapor deposition technique. The CH_4 flow rate, H_2 flow rate, chamber pressure, growth temperature, and growth are 0.5 sccm, 500 sccm, 80 Torr, 900-940 ºC, and 1.5 hours, respectively.

(2) The H-diamond is etched under O_2 atmosphere by capacitive coupled plasma reactive ion etching system in order to form the mesa-structure. Then, ohmic contact metals such as Pd, Pt, and Au are evaporated on the H-diamond using an E-gun evaporator. Lastly, Ohmic contact metals are annealed using a rapid thermal annealing system. The surface morphology and contact resistance for the metal/H-diamond will be investigated.

(3) After finding the best Ohmic contact metal for the H-diamond channel layer at high-temperature, we will improve the thermal stability of the H-diamond MOS capacitors and MOSFETs. The oxide insulator of SiO_2 is employed as the oxide insulators for the H-diamond MOS capacitors and MOSFETs. The SiO_x oxide insulator is deposited using the SD technique with a SiO_x buffer layer formed using an evaporation (EV) technique. The EV-SiO_x buffer layer is employed to protect hydrogen surface for the H-diamond channel from being damaged by plasma discharge during the SD-SiO_x deposition. Annealing process for the MOS electronic devices is performed at 500 ºC using a rapid thermal annealing system. Electrical properties of them are measured by a four-probe system at room temperature.

４．研究成果

(1) Thermal stabilities for Pt, Au, and Pd electrodes on the same H-diamond channel layer

Figure 1(a) shows surface morphology of three contacts on the H-diamond. The length and width for each electrode are the same of 100 μm. No electrodes are peeled-off after the formation process. A long-term annealing process is performed with annealing temperature and time of 400 °C and 8 hours, respectively. Their contact resistance (R_C) and specific contact resistivity (ρ_C) values are summarized in Figs. 1(b) and 1(c), respectively. Before annealing, good Ohmic contact properties are observed for only two contacts of Pt/H-diamond and Pd/H-diamond with their specific contact resistivity (ρ_C) values of 2.7×10^{-3} and 2.6×10^{-4} Ω cm², respectively. After the long-term annealing, all of three contacts on the H-diamond show good Ohmic contacts properties. The R_C for the Pt/H-diamond increases greatly. The ρ_C values for the Pt/H-diamond and Au/H-diamond are 3.1×10^{-2} and 4.2×10^{-4} Ω cm², respectively. They are higher than that of the Pd/H-diamond (1.1×10^{-4} Ω cm²). Therefore, the low ρ_C and good thermal stability for the Pd/H-diamond are achieved.

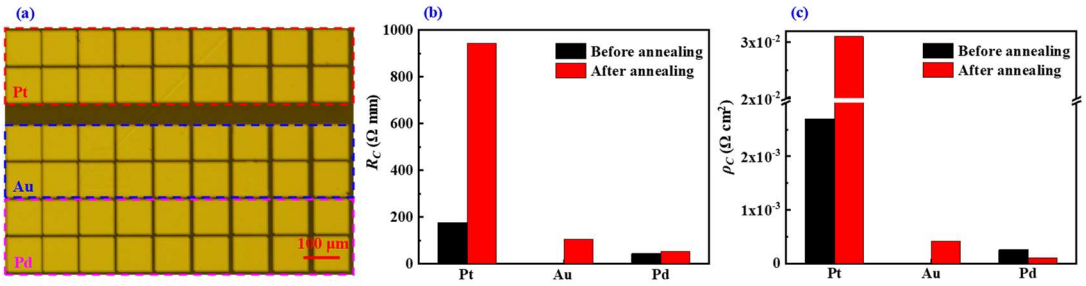

Fig. 1 (a) Surface morphologies of three contacts on the H-diamond, (b) and (c) summary of R_C and ρ_C of three contacts on the H-diamond before and after annealing, respectively.

(2) Surface morphologies of the H-diamond MOS capacitor and MOSFETs

Figures 2(a) and 2(c) show top views of the H-diamond MOS capacitor and MOSFET before annealing, respectively. Figs. 2(b) and 2(d) show top views of the H-diamond MOS capacitor and MOSFET after annealing at 500 °C for 60 min, respectively. Figs. 2(e) and 2(f) show schematic cross-sectional structures of the H-diamond MOS capacitor and MOSFET, respectively. Ohmic contact metal for the H-diamond channel is Pd with Ti/Au cover metals. Cover metals for the SiO_x gate insulators are Ti/Au bilayer. After annealing, there are still good surface morphologies for the H-diamond MOS capacitor and MOSFET.

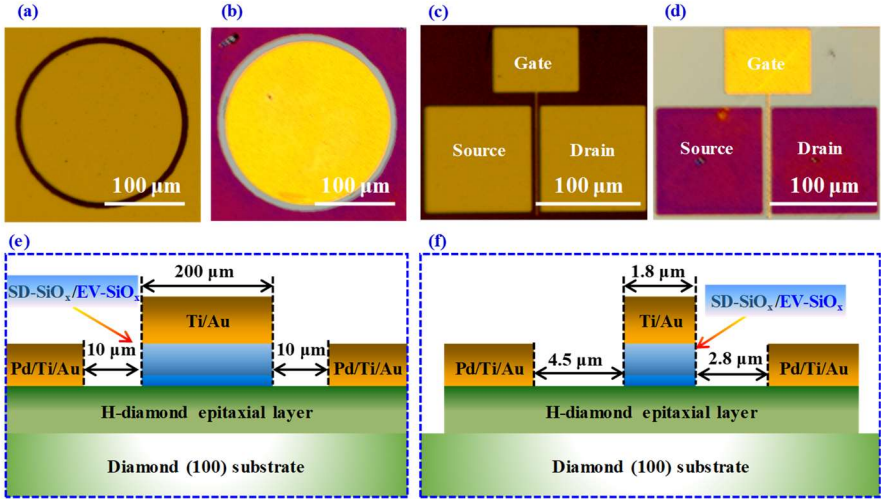

Fig. 2 ((a) and (c) Top views of the H-diamond MOS capacitor and MOSFET before annealing, respectively. (b) and (d) Top views of the H-diamond MOS capacitor and MOSFET after annealing at 500 °C for 60 min, respectively. (e) and (f) Schematic cross-sectional structures of the H-diamond MOS capacitor and MOSFET, respectively

(3) Thermal stability of the H-diamond MOS capacitors

Figures 3(a) and 3(b) show leakage current density (J) and capacitance as functions of gate voltage for the SD-SiO_x/EV-SiO_x/H-diamond MOS capacitors. The J is 1.2×10^{-5} A cm^{-2} at gate voltage of –5.0 V for the as-fabricated SD-SiO_x/EV-SiO_x/H-diamond MOS capacitor. After annealing at 500 °C for 30 and 60 min, the leakage current densities at gate voltage of –5.0 V increase to 1.6 and 0.5 A cm^{-2}, respectively, and they are around 10^{-1} A cm^{-2} at gate voltage of –3.0 V. Capacitance-voltage measurements in Fig. 3(b) for all the MOS capacitors were performed with frequency of 20 kHz. Capacitance maximum (C_{max}) for the as-fabricated SD-SiO_x/EV-SiO_x/H-diamond MOS capacitor is 0.152 μF cm^{-2} at gate voltage of –5.0 V. Dielectric constant for the SD-SiO_x/EV-SiO_x bilayer is calculated to be 4.98, which is higher than the common SiO_x film of around 3.9. With the shifts of gate voltage from 0 to –3.0 V, the C_{max} values for the MOS capacitors after annealing decrease. Before annealing, the C-V curve in the depletion region shifts to the left-hand side relative to 0 V, indicating that positive charges exist in the SD-SiO_x/EV-SiO_x bilayer. After annealing, the C-V curves in the depletion regions shift to the right-hand side relative to 0 V, which implies the existence of negative charges in the SD-SiO_x/EV-SiO_x bilayer. Capacitance as a function of measurement frequency for the SD-SiO_x/EV-SiO_x/H-diamond MOS capacitors are shown in Fig. 3 (c). The curves for the MOS capacitor before annealing is more stable than those after annealing. For all the curves, the C_{max} values start to decrease greatly at around 2×10^5 Hz.

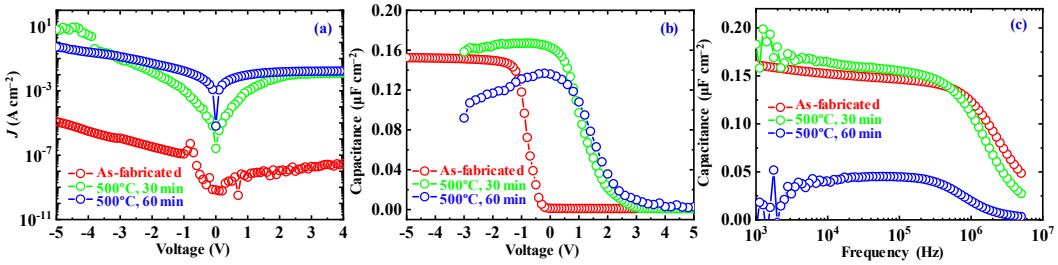

Fig. 3 (a) and (b) The J and capacitance as functions of gate voltage for the MOS capacitors before and after annealing, respectively. (c) Capacitance-frequency properties.

(4) Thermal stability of the H-diamond MOSFETs

Figures 4(a), 4(b), and 4(c) show drain-to-source current versus drain-to-source voltage (I_{DS}-V_{DS}) characteristics for the SD-SiO_x/EV-SiO_x/H-diamond MOSFETs of the as-fabricated, after annealing at 500 °C for 30 min, and after annealing at 500 °C for 60 min, respectively. Gate-to-source voltage (V_{GS}) is changed from –5.0 to 2.0 V in steps of +0.5 V for the as-fabricated SD-SiO_x/EV-SiO_x/H-diamond MOSFETs. It is changed from –3.0 to 3.0 V in steps of +0.5 V for the annealed MOSFETs. There are good operations and distinct pinch-off characteristics for all the MOSFETs. The I_{DS} maximum

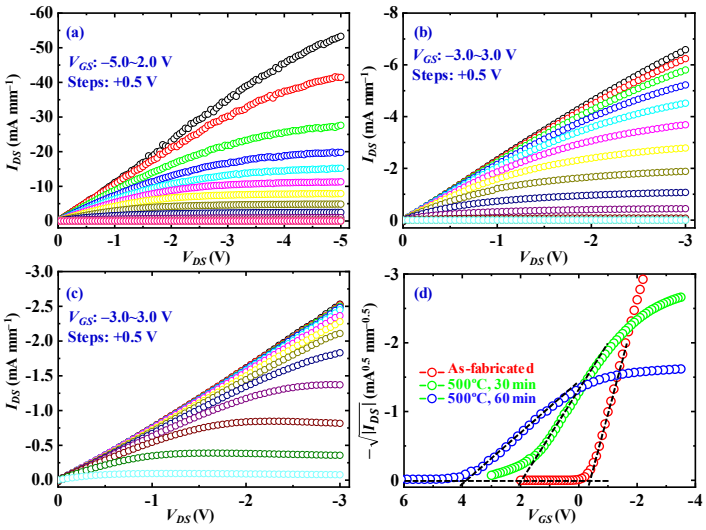

Fig. 4 (a), (b), and (c) The I_{DS}-V_{DS} characteristics for the MOSFETs of as-fabricated, after annealing at 500 °C for 30 min, and after annealing at 500 °C for 60 min, respectively. (d) The $-\sqrt{|I_{DS}|}$-V_{GS} characteristics for the H-diamond MOSFETs before and after annealing.

for as-fabricated MOSFET is –53.3 mA mm^{-1}. Those are –6.6 and –2.6 mA mm^{-1} for the MOSFETs after annealing for 30 and 60 min, respectively. On-resistances normalized the W_G for the as-fabricated H-diamond MOSFETs are 93.6 and 149.1 Ω mm at the V_{GS} of –5.0 and –3.0 V, respectively. Those for the annealed MOSFETs are 441.9 and 1234.6 Ω mm at the V_{GS} of –3.0 V, respectively. Annealing makes the decrease of hole density in the H-diamond channel layer, leading to the low I_{DS} maxima and high on-resistances. Fig. 4(d) shows $-\sqrt{|I_{DS}|}$-V_{GS} characteristics to determine threshold voltage (V_{TH}) values of the MOSFETs. For the as-fabricated SD-SiO_x/EV-SiO_x/H-diamond MOSFET, the V_{TH} is –0.4 ±0.1 V. After annealing at 500 °C for 30 and 60 min, the V_{TH} values change to be 1.9 ±0.1 and 3.8 ±0.1 V, respectively. Annealing makes the MOSFET vary from normally-off to normally-on characteristics.

Figures 5(a) and 5(b) show log|I_{DS}| versus V_{GS} characteristics for the MOSFETs before and after annealing at 500 °C for 60 min, respectively. On/off ratio and SS for the as-fabricated SD-SiO_x/EV-SiO_x/H-diamond MOSFETs are 1.4 × 10^9 and 88 mV dec^{-1}, respectively. After annealing, they change to 1.4 × 10^4 and 530 mV dec^{-1}, respectively. According to relationship between SS and interfacial trapped charge density (D_{it}) for the oxide/H-diamond heterojunctions, the D_{it} value for the as-fabricated SiO_x/H-diamond interface can be calculated to be 4.6 × 10^{11} eV^{-1} cm^{-2}. Since the C_{max} for SD-SiO_x/EV-SiO_x/H-diamond MOS capacitor after annealing at 500 °C for 60 min is in the range of 0.045~0.137 μF cm^{-2}, the D_{it} value for the annealed SiO_x/H-diamond interface can be calculated in the range of 2.2~6.8 × 10^{12} eV^{-1} cm^{-2}.

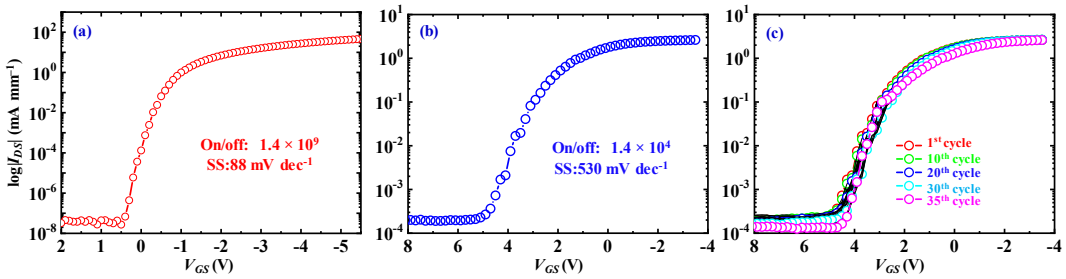

Fig. 5 (a) and (b) The log |I_{DS}|–V_{GS} characteristics for the MOSFETs of as-fabricated and after annealing at 500 °C for 60 min, respectively. (c) The log |I_{DS}|–V_{GS} characteristics for the annealed MOSFET with 35 cycles repeat measurements.

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３．学会等名
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４．発表年
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１．発表者名
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〔図書〕　計0件

〔産業財産権〕

〔その他〕
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