【Grant-in-Aid for Scientific Research (S)】

Broad Section C

# Title of Project : Development of a germanium spin MOSFET

HAMAYA, Kohei
(Osaka University, Graduate School of Engineering Science, Professor)

Research Project Number : 19H05616 Researcher Number : 90401281
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## 【Purpose and Background of the Research】

Semiconductor electronics has brought us technological innovation in the field of information industries. From now on, the further developments of semiconductor technologies will become the core of the industries in artificial intelligence, IoT devices, and some related technologies. In recent years, for high speed operation and low power dissipation, novel semiconductor devices are strongly required. One of the key devices is the spin MOSFET, which was proposed by Sugahara and Tanaka, as schematically shown in Fig.1. If one can realize the high-performance spin MOSFET on the Si platform, the nonvolatile memory devices can be integrated into the CMOS transistors. By using Ge channel and S/D contacts without using insulator tunnel barriers, scalable spin MOSFETs with ultra-low power consumption, reducing the parasitic resistance between S/D contacts, will be developed.

For that reason, we have so far developed a new spin injection technology for Ge (SiGe) with using ferromagnetic Heusler alloy and without using insulator tunnel barriers at the S/D contacts, as shown in Fig. 1. In this project, we will further enhance the spin injection efficiency without using insulator tunnel barriers. Also, we will develop some of important Ge technologies for channel and gate-stack structures. As a result, we would like to develop a Ge-MOSFET device with nonvolatile memory effect (high MR ratio) and low-power current switching (on/off operation) at room temperature.

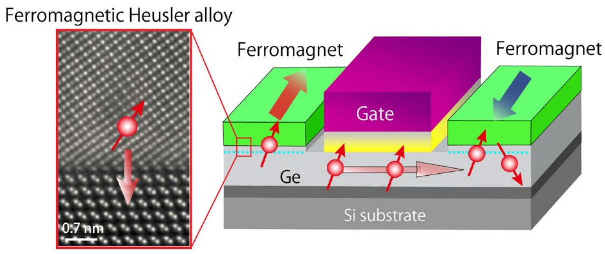


Fig.1. Schematic of spin MOSFET (right) and TEM image of a ferromagnetic Heusler alloy/Ge interface (left).

## 【Research Methods】

In this research project, we focus on the following four experiments. First, we study high-quality formation technologies of ferromagnetic Heusler alloy/Ge heterointerfaces for enhancing spin injection efficiency at room temperature. Second, we study new Ge (SiGe) channel structures for suppressing spin relaxation at room temperature even on a Si platform. Third, we have to develop low-temperature gate-stack fabrication processes for Ge spin MOSFET with a top-gate structure. Finally, we will develop a specialized microfabrication process for integration of the above technologies for operation of Ge spin MOSFET.

## 【Expected Research Achievements and Scientific Significance】

From the above research and developments, we will simultaneously perform a highly-enhanced MR ratio and low-power current switching (on/off operation) at room temperature in Ge-MOSFET structures. This project will demonstrate an integration of nonvolatile memory effect with high-performance semiconductor devices. The developed Ge spin MOSFET will contribute to some of novel technologies with high speed operation and low power consumption for artificial intelligence, IoT devices, and some related technologies in future.

## 【Publications Relevant to the Project】

・M. Yamada, M. Tsukahara, Y. Fujita, T. Naito, S. Yamada, K. Sawano, and K. Hamaya, "Room-temperature spin transport in *n*-Ge probed by four-terminal nonlocal measurements", Appl. Phys. Express **10**, 093001 (2017).
・K. Hamaya, Y. Fujita, M. Yamada, M. Kawano, S. Yamada, and K. Sawano, "Spin transport and relaxation in germanium (Topical Review)", J. Phys. D: Appl. Phys. **51**, 393001 (2018).

## 【Term of Project】 FY2019-2023

## 【Budget Allocation】 155,500 Thousand Yen

## 【Homepage Address and Other Contact Information】

http://www.semi.ee.es.osaka-u.ac.jp/hamayalab/
hamaya@ee.es.osaka-u.ac.jp