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研究課題名（和文）HARFSR: A Hardware-Accelerated Real-time Sound Field Rendering System for Large-scale Sound Environments

研究課題名（英文）HARFSR: A Hardware-Accelerated Real-time Sound Field Rendering System for Large-scale Sound Environments

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交付決定額（研究期間全体）：（直接経費）　　3,200,000円

研究成果の概要（和文）：リアルな音の伝播は、ユーザーの臨場感を大きく向上させ、人とコンピューターのインタラクション、リアルなコミュニケーションに不可欠である。本研究では、アルゴリズムとアーキテクチャの協調設計により、ハードウェアで高速化された音場レンダリングシステムを検討し、アーキテクチャの拡張を探り、他領域の音波伝搬問題を解決するための汎用的な高速化プラットフォームを構築した。計算量とメモリ使用量を削減するために、新しいレンダリングアルゴリズムを研究され、計算を高速化するための革新的なアクセラレータシステムを開発した。それで、大規模な音響環境で高忠実度な聴覚を実現する技術を探った。

研究成果の学術的意義や社会的意義
大規模な音空間における音場レンダリングは計算負荷が高く、リアルタイムアプリケーションからオフラインアプリケーションまで多くのアプリケーションで重要である。本研究の成果は、高忠実度の聴覚を実現する音場レンダリングのソリューションを提供し、人間中心のコンピューティングの最先端技術を推進する。また，本研究の成果を発展させることで，バーチャルリアリティやヒューマンコンピュータのインタラクティブの新しい技術を創出する可能性がある。

研究成果の概要（英文）：Realistic sound propagation significantly improves the sense of presence of users, and it is indispensable in human-computer interaction and realistic communication. This research investigated a hardware-accelerated sound field rendering system by co-designing algorithm and architecture, and explored the architecture extension to investigate a generic accelerated platform to solve sound/wave propagation problems in other domains. The new rendering algorithm was studied to reduce computations and memory demands, and the novel accelerated system was developed to speed up computations. In addition, the technology of achieving high-fidelity auditory perception in large-scale sound environments was explored.

研究分野：Information System

キーワード：Sound field rendering　FPGA　FDTD　room acoustics

１．研究開始当初の背景

Realistic sound propagation can significantly improve the sense of presence and immersion of users, augment the visual sense and situational awareness of users, and it is indispensable in human-computer interaction and realistic communication. Sound field rendering exhibits numerical methods to model sound propagation in spatial and time domains, and it is fundamental to numerous scientific and engineering applications. To date, geometric methods and wave-based methods have been proposed to analyze sound wave propagation. In particular, wave-based methods has widely applied because of their high accuracy. Since spatial grids are usually oversampled to suppress the dispersion errors in wave-based methods, the additional computational cost is incurred significantly. Given the auditory range of humans (20Hz-20kHz), analyzing sound wave propagation in a space corresponding to a concert hall or a cathedral (e.g. 10000m^3) for the maximum simulation frequency of 20kHz requires petaflops of computing power and terabytes of memory. Currently, only supercomputers or large computer clusters can achieve such performance, but they are prohibitively expensive. Therefore, (1) reducing the oversampling and dispersion errors in algorithm and accelerating computations using specific hardware are necessary; (2) investigating sound rendering system with dedicated hardware acceleration is dispensable.

On the other hand, the computing landscape has shifted towards heterogeneous systems with general-purpose graphic processing units (GPGPUs) or field programming gate arrays (FPGAs) to speed up computation in recent years. Compared with GPGPUs, FPGAs are more attractive for real-time sound field rendering because of their re-programmability and customization, which make it possible to tailor input/output interfaces and system data path according to data flows in applications. This research will investigate an FPGA-based real-time sound field rendering system to achieve high-fidelity auditory perception in large-scale sound environments.

２．研究の目的

This research will investigate three specific topics towards developing a real-time sound field rendering system, and a virtual concert hall will be developed as a real demonstration to verify the propose and explore the high-fidelity auditory perception technology.

Aim 1: New hardware-oriented and low-dispersion rendering algorithm to reduce computations and memory demands.

Aim 2: Novel hardware-accelerated system to speed up computation.

Aim 3: Extension of the proposed system and developing a generic hardware platform to solve wave/sound propagation problems.

３．研究の方法

Aim 1: New hardware-oriented and low-dispersion rendering algorithm to reduce computations and memory demands.

The FDTD algorithm were focused due to its high accuracy, ease of implementation and parallelization. The FDTD schemes with higher-order accuracy in space and time domains for 2D and 3D spaces were derived, analyzed, and compared to investigate the accurate, efficient, and easy hardware implementation schemes. Their numerical stability was analyzed using frequency-domain analysis, the order of accuracy was compared, and the required hardware resources were estimated.

Aim 2: Novel hardware-accelerated system to speed up computation.

(1) system decomposition and parallelism. The system decomposition methods were compared and studied. The spatial parallelism was proposed to speed up computation and save required memory bandwidth, in which a sound space was divided into sub-sound-spaces, and a sliding window-based data buffering system was applied to alleviate the required memory bandwidth. The temporal parallelism was investigated to reuse data and reduce data accesses to external memory.
(2) system specification and verification. Data flow in the proposed FDTD algorithm was analyzed and system architecture was specified, in which spatial blocking and temporal blocking were applied to reduce required memory bandwidth and reuse data, respectively. A simulator was developed using C programming language to verify system function, locate the performance bottleneck, find and fix the functional failures of the hardware system in advance.

(3) development and evaluation of prototype machine. A prototype machine was designed using OpenCL programming language. The co-design and co-verification of the hardware prototype and the cycle-accurate simulator were employed to verify and optimize the hardware system. The performance of the prototype machine, such as hardware resource utilization, computation time, computational throughput, was evaluated in the case of different application scenarios. As a comparison, the related software-based simulation systems were developed using C++ programming language and performed on a desktop machine with 512 GB DDR4 RAMs and a Xeon Gold 6212U processor (24 cores) running at 2.4 GHz.

(4) development of virtual concert hall. Sound filed propagation in a virtual three-dimensional sound space with dimension being 16m × 8m × 8m was analyzed by the proposed sound field rendering system implemented using the FPGA card DE10-Pro. An impulse signal was as an incidence to the system, and the computation time, sampling rate, and computational throughput were measured in the case of different rendering algorithms.

Aim 3: Extension of the proposed system and developing a generic hardware platform to solve wave/sound propagation problems. In principle, the computation of the FDTD-based wave equation was stencil computation. Systolic array and coarse-grained reconfigurable architecture (CGRA) were explored to develop a generic hardware-accelerated platform for wave propagation problems. The related simulators were developed, system prototypes were investigated and simulated to verify the design, and their performance was evaluated in the case of different architectural parameters.

４．研究成果

Aim 1: New hardware-oriented and low-dispersion rendering algorithm to reduce computations and memory demands.

A high-order FDTD method was developed to reduce the memory requirement by applying the high-order Lagrange polynomial fitting approximation in the spatial domain and second-order central difference approximation in the time domain. The high-order FDTD method only introduced the neighbor grids along the axes. To analyze sound field propagation in a shoebox with dimension being 8m × 8m × 7m, compared with the 2^{nd}-order FDTD scheme, the 6^{th}-order and 4^{th}-order FDTD schemes reduced 46% and 35% of memory requirement, respectively. On the other hand, when the order of FDTD scheme was increased, since more neighbor grids were involved in computation, the number of operations and memory accesses were increased. In the 2^{nd}-order scheme, sound pressures of a grid and its six neighbor grids at previous time steps were required to calculate its sound pressure. In contrast, sound pressures of a grid and its 18 neighbor grids were needed to compute its sound pressure in the 6^{th}-order scheme.

Aim 2: Novel hardware-accelerated system to speed up computation.

(1) Rendering system with the 2^{nd}-order FDTD scheme

An FPGA-based sound field rendering system with the 2^{nd}-order FDTD scheme was firstly developed and implemented using the FPGA card DE5a-NET, in which spatial parallelism was employed to reduce the required memory bandwidth and the size of on-chip buffers. In order to efficiently utilize the external memory bandwidth and speed up computation, data accesses were coalesced and computation was vectorized simultaneously by loop unrolling. Furthermore, shift registers were used as on-chip buffers to exploit the regular memory access pattern. The system performance was evaluated in the case of the layer size being 128 × 128 to 256 × 256 and the number of grids computed in parallel being 4, 8, 16, 32, 64, 128, respectively. Compared to the software simulation performed on a desktop machine with 128 GB DDR4 RAMs and an Intel i7-7820X processor running at 3.6 GHz, the proposed FPGA-based accelerator achieved up to 2.98 times in computing performance in the case of different layer sizes and different number of grids computed concurrently even though the FPGA system ran at about 267 MHz.

(2) Rendering system with the high-order FDTD scheme

The sound field rendering systems with the 2^{nd}-order, 4^{th}-order, and 6^{th}-order FDTD schemes were designed using OpenCL programming language and implemented using the FPGA card DE10-Pro, which contained a Stratix 10 SX FPGA (1SX280HU2F50E1VG) and 8 GB on-board DRAMs. Except for the spatial parallelism, the temporal parallelism was introduced to reuse data and reduce data accesses to external memory. As shown in Fig. 1, 16 processing elements (PEs) were cascaded to compute sound pressures of grids of a same spatial block at continuous 16 time steps. Table 1 presented the hardware resource utilization when the size of spatial block

was 128 × 128, the number of PEs was 16, and the number of grids computed concurrently was 16. To analyze sound propagation in a three-dimensional sound space with dimension being 16m × 8m × 8m, the proposed FPGA-based sound field rendering systems speeded up computation by 11 times, 13 times, and 18 times in the 2nd-order, 4th-order, and 6th-order FDTD schemes, respectively, over software simulations carried out on a desktop machine with 512 GB DRAMs and an Intel Xeon Gold 6212U processor running at 2.4 GHz. The computational throughput and sampling rate of the output sound were also increased significantly in the developed rendering system. All these results demonstrated that the proposed solution, including algorithm, architecture, and design, was reasonable and feasible to achieve high-fidelity auditory perception in large- scale sound environment.

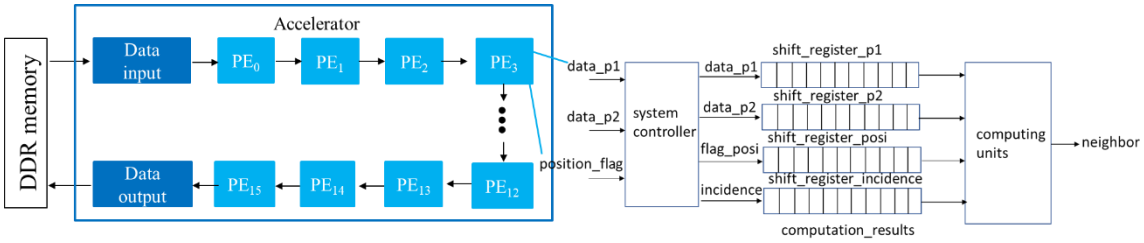

Fig. 1 System architecture

Table 1. Hardware Resource Utilization

Orders	Logic Utilization	DSP Blocks	RAM Blocks	Clock Frequency (MHz)
2nd	269,159 (29%)	342 (6%)	1,785 (15%)	357
4th	293001 (31%)	630 (11%)	3764 (32%)	355
6th	335,237 (36%)	918 (16%)	4,309 (37%)	337

Aim 3: Extension of the proposed system and developing a generic hardware platform to solve wave/sound propagation problems.

The systolic architecture and CGRA were studied to develop a generic hardware system for stencil computation, which was the computation pattern of wave/sound propagation with FDTD method. The architecture of PEs in the systolic architecture was simply changed according to wave equations and the system could solve wave/sound propagation problems in different applications. The CGRA with embedded routers and CGRA with discrete routers were investigated. In the CGRA system, the stencil patterns in different wave/sound propagation problems were compiled by a compiler to generate data flow graph and inputted to the CGRA to compute directly.

５．主な発表論文等

〔雑誌論文〕　計1件（うち査読付論文　1件／うち国際共著　1件／うちオープンアクセス　0件）

１．著者名 Yiyu Tan, Toshiyuki Imamura, and Masaaki Kondo	４．巻 69
２．論文標題 FPGA-based Acceleration of FDTD Sound Field Rendering	５．発行年 2021年
３．雑誌名 Journal of the Audio Engineering Society	６．最初と最後の頁 542-556
掲載論文のDOI（デジタルオブジェクト識別子） 10.17743/jaes.2021.0025	査読の有無 有
オープンアクセス オープンアクセスではない、又はオープンアクセスが困難	国際共著 該当する

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〔図書〕　計0件

〔産業財産権〕

〔その他〕

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６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考

７．科研費を使用して開催した国際研究集会

〔国際研究集会〕　計0件

８．本研究に関連して実施した国際共同研究の実施状況

共同研究相手国	相手方研究機関