様　式　Ｃ－１９、Ｆ－１９－１、Ｚ－１９　（共通）

科学研究費助成事業　　研究成果報告書

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研究課題名（和文）Intelligent Active Balancing of Parallel/Series-connected Power Devices

研究課題名（英文）Intelligent Active Balancing of Parallel/Series-connected Power Devices

研究代表者
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交付決定額（研究期間全体）：（直接経費）　　3,300,000円

研究成果の概要（和文）：The active gate delay control is implemented for the SiC power devices as well as the IGBT power devices. The active gate control strategy is employed under the dynamic operation of the device that is turn-on and turn-off. A parallel hybrid switch is developed with gate driver and inbuilt delay.

研究成果の学術的意義や社会的意義
The electrification is necessary to tackle the problem of CO2 emission. The paralleling of the devices are used in high power converters for electrification, the current unbalancing problems addressed in this research will help to create an understanding and possibly provide a solution.

研究成果の概要（英文）：The active gate control is employed for the parallel-connected power semiconductor devices and current unbalancing is minimized using active gate control methodology. This active gate delay control is implemented for the SiC power devices as well as the IGBT power devices. The active gate control strategy is employed under the dynamic operation of the device that is turn-on and turn-off. Further the research analysis is performed on the gate signal characteristic study corresponding to the active gate control. The correlation between the device current unbalancing and Miller plateau is realized. A parallel hybrid switch is developed with specific gate driver and inbuilt delay for the appropriate hybrid switching.

研究分野：Power Electronics System and Control

キーワード：Power device　Gate Driving Control　Parallel-connection　Current balancing　Power converter

１．研究開始当初の背景

(1) The power devices development has made a leap in the performance and system rating since its inception. However, the horizon for operating range of a single device considering blocking voltage and current capability is constrained by different factors such as yield and manufacturing process issues. And the devices are required to connect in parallel to match desired current rating for many applications such as electric vehicles (EV) and wind power generations.

(2) There is a fundamental issue involved with paralleling of the devices, that is current unbalancing. The current unbalancing issue creates severe long-term concerns such as system derating, thermal derating and reliability issues. Enhancement and optimization of the performance of power semiconductor devices are of fundamental concern, especially for the system consisting of parallel-connected devices.

２．研究の目的

(1) The understanding of current unbalancing for the parallel-connected power semiconductor devices under dynamic operating condition.

(2) The effect of unbalancing on gate voltage waveform and develop an understanding of the gate driving techniques as well as current balancing techniques.

(3) The gate control to minimize and/or mitigate current unbalancing during dynamic operation.

３．研究の方法

(1) The individual gate driving units for the corresponding device to control the gate signals independently using the delay control technique. In addition, the effect of delay control on the gate voltage waveform and required resolution for the delay corresponding to unbalancing.

(2) The hybrid paralleling of the devices to realize a hybrid switch to realize an improved system performance.

４．研究成果

(1) The gate driving techniques and current balancing techniques are categorized and reviewed for the parallel-connected power devices. Furthermore, the gate delay control corresponding to different feedback parameters are surveyed that can be categorized as direct and indirect active gate delay control Figure 1 and Figure 2.

(2) The unbalancing phenomenon for parallel connected IGBT devices is realized using the unequal gate resistance for dynamic operation. The gate delay feedback control minimizes the unbalancing during turn-on and turn-off independently. The impact of unbalancing and gate delay control on gate voltage waveform was substantiated that provides the information about the impact on Miller plateau.

(3) The unbalancing phenomenon for parallel connected SiC devices was researched considering the dynamic current unbalancing and a delay control is employed that minimized the dynamic current unbalancing.

(4) The hybrid switch considering the SiC-GaN is developed with a specific gate drive design for the switching paralleled hybrid SiC-GaN switch. And a buck converter is developed using parallel hybrid switch to investigate the switching performance.

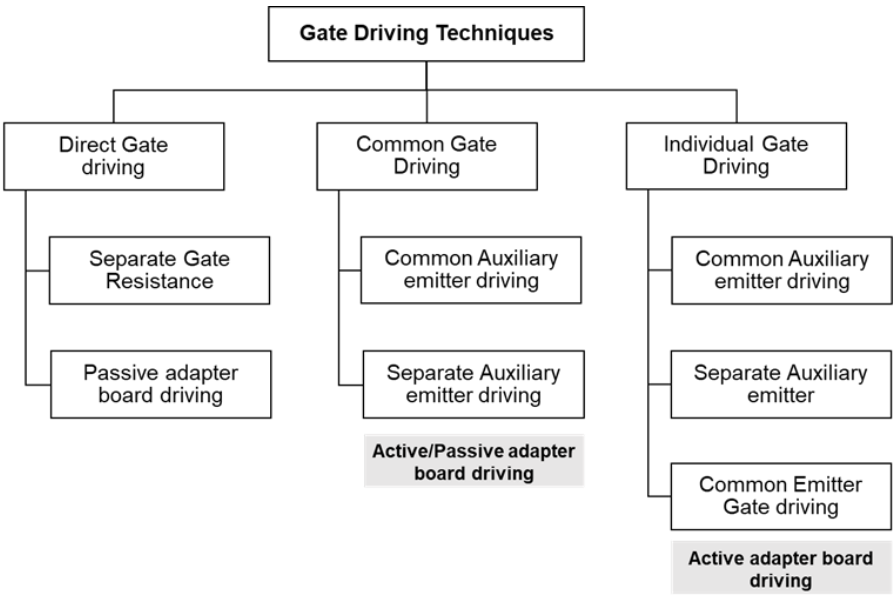

Figure1. Gate-driving techniques for parallel-connected power devices.

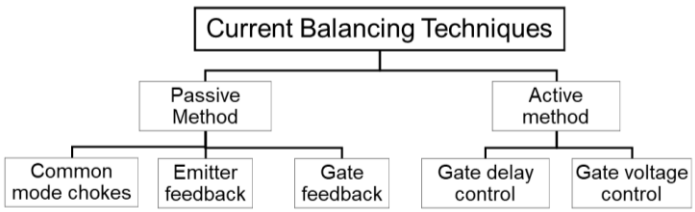

Figure2. Gate delay control techniques for parallel-connected power devices.

全論文リスト

1. Ravi Nath Tripathi, Ichiro Omura, "Paralleling of IGBT Power Semiconductor Devices and Reliability Issues", *Electronics*, 12(18), 2023, 3826 (19 pages). DOI: 10.3390/electronics12183826 【査読有】【責任著者】
2. Ravi Nath tripathi, Ichiro Omura, "並列 IGBT デバイスの電流均一化のためのゲート遅延制御とミラープラトー効果", *電気学会電子デバイス・半導体電力変換合同研究会*, Fukuoka, Japan, 2023, pp. 47-52. DOI: https://www.bookpark.ne.jp/cm/ieej/detail/IEEJ-20231027X02901-009-PDF/ 【査読なし】【責任著者】
3. Ravi Nath Tripathi, "Current Balancing of Parallel-Connected SiC devices using Active Gate Control", *Proc. of 25th International Conference on Electrical Machines and Systems (ICEMS),* Chiang Mai, Thailand, 2022, pp. 1-5.

DOI: 10.1109/ICEMS56177.2022.9983228 【査読有】【責任著者】

4. B. Battuvshin, Ravi Nath Tripathi, Ichiro Omura, Alberto Castellazzi, "Hybrid GaN-SiC Power Switches for Optimum Switching, Conduction and Free-Wheeling Performance", *Proc. of 34th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2022*, Vancouver, Canada, 2022, pp. 301-304.
DOI: 10.1109/ISPSD49238.2022.9813667 【査読有】

５．主な発表論文等

〔雑誌論文〕　計1件（うち査読付論文　1件／うち国際共著　0件／うちオープンアクセス　1件）

１．著者名 Tripathi Ravi Nath、Omura Ichiro	４．巻 12
２．論文標題 Paralleling of IGBT Power Semiconductor Devices and Reliability Issues	５．発行年 2023年
３．雑誌名 Electronics	６．最初と最後の頁 3826～3826
掲載論文のDOI（デジタルオブジェクト識別子） 10.3390/electronics12183826	査読の有無 有
オープンアクセス オープンアクセスとしている（また、その予定である）	国際共著 －

〔学会発表〕　計3件（うち招待講演　0件／うち国際学会　2件）

１．発表者名 Ravi nath Tripathi
２．発表標題 Current Balancing of Parallel-Connected SiC devices using Active Gate Control
３．学会等名 IEEE-ICEMS 2022（国際学会）
４．発表年 2022年

１．発表者名 Battuvshin Bayarkhuu
２．発表標題 Hybrid GaN-SiC Power Switches for Optimum Switching, Conduction and Free-Wheeling Performance
３．学会等名 IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)（国際学会）
４．発表年 2022年

１．発表者名 Ravi nath Tripathi
２．発表標題 Gate Delay Control for Current Equalization of Parallel IGBT Devices and Miller Plateau Effect
３．学会等名 電気学会電子デバイス・半導体電力変換合同研究会
４．発表年 2023年

〔図書〕　計0件

〔産業財産権〕

〔その他〕

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６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考

７．科研費を使用して開催した国際研究集会

〔国際研究集会〕　計0件

８．本研究に関連して実施した国際共同研究の実施状況

共同研究相手国	相手方研究機関