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研究課題名（和文）Research on Distributed Millimeter-Wave Phased-Array Transceiver

研究課題名（英文）Research on Distributed Millimeter-Wave Phased-Array Transceiver

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交付決定額（研究期間全体）：（直接経費）　　3,500,000円

研究成果の概要（和文）：本研究は低コスト、再構成可能なミリ波フェーズドアレイ無線送受信機回路を提案する。従来の大規模、中心化フェーズドアレイと比べ、提案手法はよりフレキシブルな運用ができる。本研究は双方向技術及びドハティPAを提案し、送受信機回路面積の削減および効率の向上を実現する。同時に、本研究は位相誤差補償回路及び校正回路を提案し、フェーズドアレイの移相誤差及び振幅誤差を抑え、不要波の発射を低減する。

研究成果の学術的意義や社会的意義
The millimeter-wave phased-array is significant in wireless communication. However, conventional centralized phased-arrays cannot deal with the complex environments. In this research, the distributed phased-array transceivers are proposed with less cost and compact size.

研究成果の概要（英文）：This research introduces low-cost, reconfigurable mmW distributed phased-array transceivers. The deployment of such arrays is much more flexible compared with centralized arrays. To realize compact, low-cost characteristics, this research introduces the neutralized bi-directional architecture. The phased-array gain and stability are enhanced with a minimized area and cost. To maintain high-efficiency characteristics, this research explores Doherty PA with higher efficiency at backoff. To minimize the unwanted radiation, this research first introduces a phase shifter with phase compensation network. The errors are therefore reduced. Furthermore, this research introduces on-chip magnitude and phase detection circuits for correcting the errors between channels.

研究分野：Silicon-based mmW phased-array transceiver

キーワード：mmW　transceiver　phased-array　cmos　wireless　5G　B5G

様　式　Ｃ－１９、Ｆ－１９－１、Ｚ－１９（共通）

１．研究開始当初の背景

The perpetual rise in data traffic, primarily driven by the introduction of advanced technologies like 5G, IoT, and AI, necessitates the expansion of communication bandwidth. Nonetheless, the existing microwave band has already reached its limits owing to the extensive array of applications it currently supports. Considering this background, the millimeter-wave (mmW) band with ample frequency resources assumes a central role in shaping the future landscape of wireless communications.

To extend the communication range of mmW transceivers, the beamforming technique in conjunction with phased-array implementation becomes imperative. By augmenting the number of phased-array antennas, directional beams can be precisely formed, targeting specific positions. Consequently, the utilization of beamforming technique assumes critical significance in enabling the transmission of ultra-fast mmW data streams.

Conventionally, the large-sized centralized phased-arrays consisting of over 64 element-transceivers are utilized for generating highly directional mmW beams, which cannot deal with the complex urban environments. In this research, the mmW distributed phased-array transceivers with much less element-transceivers are proposed. Different from the conventional centralized phased-array transceivers, multiple distributed arrays will work together to focus the mmW data beam towards the user device. The distributed arrays are also with less manufacturing cost and compact size. Therefore, the deployment of distributed arrays becomes much more flexible. Street lights, moving vehicles, and even human beings could be equipped with such compact arrays.

２．研究の目的

This research aims at realizing CMOS mmW distributed phased-array transceivers. The designed phased-array transceiver should obtain compact, low cost, high-efficiency, and high data rate characteristics. Also, the undesired radiation of the distributed phased-array transceivers should be minimized at unwanted directions for less blocker generations.

３．研究の方法

(1) To realize compact, low-cost characteristics for the distributed phased-array transceivers, this research introduces the bi-directional architecture. The transmission path and the reception path of the phased-array channels are combined for a compact chip area and a minimized cost. A neutralized bi-directional architecture is further proposed. The amplifier gain and the stability are enhanced in the proposed distributed phased-arrays.
(2) To maintain high-efficiency characteristics for the distributed phased-array transceivers, this research explores the Doherty PA. In 5G/B5G, the OFDMA-mode signals are usually used. The PAPR of such signals is usually high and degrade the efficiency of the transceivers. The Doherty PA can improve the PAE of PA at backoff.
(3) To minimize the unwanted radiation of the distributed array, this research first introduces a switch-type phase shifter with low gain and phase errors. A high-pass phase compensation network is utilized to improve the errors of the phase shifter. Furthermore, this research also introduces an on-chip magnitude and phase detection circuit for detecting the gain and phase errors between different transceiver paths. The radiated signal from each path will be down-converted and detected by the proposed circuit. High detection accuracy and low power consumption can be maintained by this research.

４．研究成果

This section will introduce the achieved results in detail:

[成果 1]

The distributed mmW phased-array is designed to support data rate with multiple Gbps. Besides, the system size of the distributed phased-arrays should be compact enough. The system cost should also be minimized for easy deployment. Therefore, a neutralized bi-directional technique is proposed in this research and applied to the phased-array transceiver. Fig. 1 shows the block diagram of the proposed phased-array transceiver at 39GHz band:

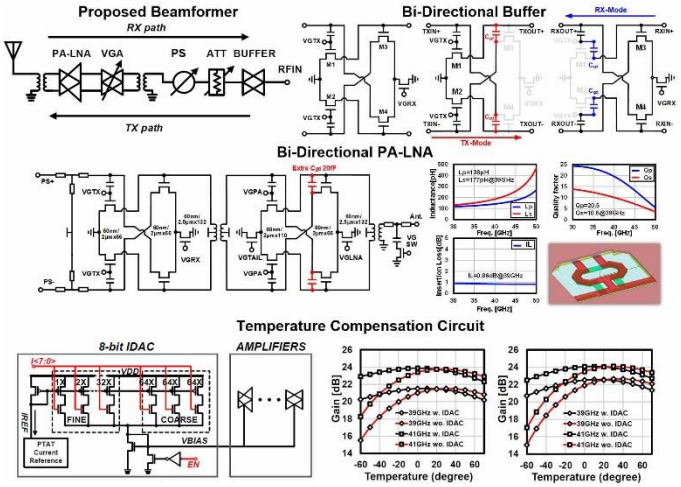

Fig. 1 Proposed bi-directional beamformer and temperature compensation circuits. **[成果 1]**

The proposed transceiver is capable of operating in TX and RX modes with the same bi-directional circuit chain. A single-element transceiver consists of a 2-stage PA-LNA, an VGA, an attenuator, a phase shifter, and an isolation buffer.

Fig. 1 also shows the detailed circuit of the neutralized bi-directional the bi-directional amplifiers are designed based on the proposed neutralized bi-directional core. Compared with the conventional switch-based bidirectional approach, the proposed bi-directional amplifier completely shares the inter-stage matching networks between the TX and the RX. Thus, the required on-chip area is further minimized. The proposed neutralized bi-directional core can also realize cross-coupling capacitor neutralization in both TX and RX modes. The higher gain characteristics and the enhanced reverse isolation are realized by the proposed bidirectional amplifier, which contributes to low-noise and high-stability operation as well as an improved phase tuning isolation.

Due to the different transistor size requirements for PA and LNA, an unbalanced bidirectional amplifier architecture is proposed. Extra capacitors Cgd are attached to the LNA transistor to compensate the additional Cgd from the PA transistor. As a result, neutralization can be realized in both operation modes. The PA and LNA share the antenna node with a switching capacitor. By switching the transistor, the output matching network can be adapted to the required impedance for PA and LNA. At 39GHz, this work can achieve 15.6dBm output power in TX mode and 5-dB NF in RX mode. Please note this result is realized with the TRX switch.

[成果 2]

The phase shifting performance is critical for distributed phased-array transceivers. The phase error and gain error will cause misalignment between different distributed transceiver cells. Therefore, this research also explores the method for minimizing the phase and gain errors. A configuration of a phase compensation network is adopted. It utilizes characteristics of high/low-pass filters to compensate for phase error over frequencies as well as phase states. The proposed phase shifter exhibits RMS group delay of less than 3.8ps, and low RMS phase and gain errors of 3.9degree and 2.2dB from 19 to 34GHz, respectively:

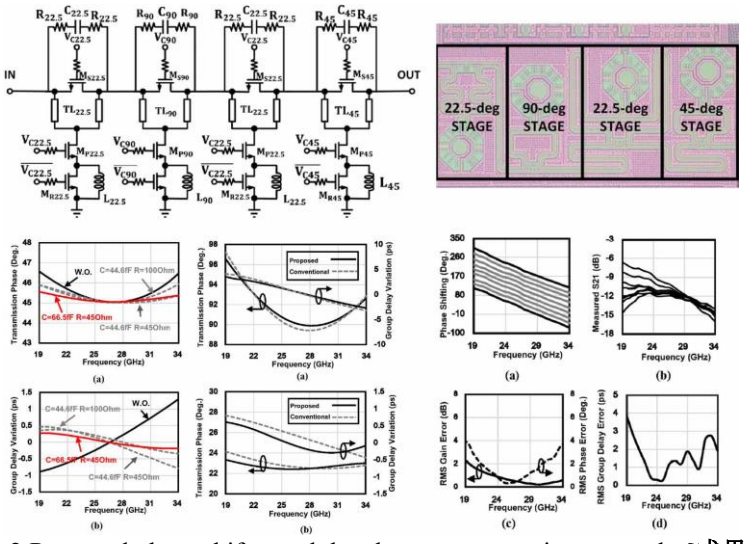

Fig. 2 Proposed phase shifter and the phase compensation network. **[成果 2]**

The conventional circuit schematic of bridged-T STPS can be configured between the bypass state and the phase-delay state. In order to achieve low phase error, the slope of the phase with respect to frequency (group delay) in the phase-delay state and the bypass state should be equal. The phase-delay state presents phase-lagging to the reference phase, which introduces large group delay imbalance between the two states. To deal with this issue, we use a high-pass filter for the phase compensation. Using the phase-leading characteristic of a high-pass filter, the proposed STPS can realize low phase error with extended operating bandwidth.

The proposed STPS can achieve 180degree phase shifting with a 22.5degree step. The inductors are partly placed by transmission lines (TL) considering large size and parasitic capacitance. The proposed phase shifter is fabricated using 65-nm CMOS process. The core area of the design is 0.13mm^2. The right bottom corner of Fig. 2 shows the measured phase shifting. The whole design covers 180degree with 22.5-degree resolution from 19 to 34GHz. The measured insertion loss is 11.2dB with 0.4dB gain variation at 27GHz, respectively. The maximum insertion loss is 16.1dB over the whole bandwidth. The measured maximum RMS phase and gain errors are 3.9degree and 2.2dB from 19 to 34GHz. At 27GHz, the phase and gain errors are 0.45degree and 0.46dB, respectively. The achieved RMS group delay error is less than 3.8ps within the operating bandwidth.

[成果 3]

To further improve the transceiver efficiency, this work also explores the Doherty PA technique in silicon-based technique. In 5G, the high peak-to-average power ratio (PAPR) of 5G OFDMA-mode modulated signal limits the transmitter to operate at 6-dB or even more back-off point. As the key component of the phased-array transmitter, the power-efficient PA with sufficient output power and good linearity performance is required. This work focuses on the n259 band PA design. Fig. 3 shows the proposed Doherty PA design and the corresponding measurement results.

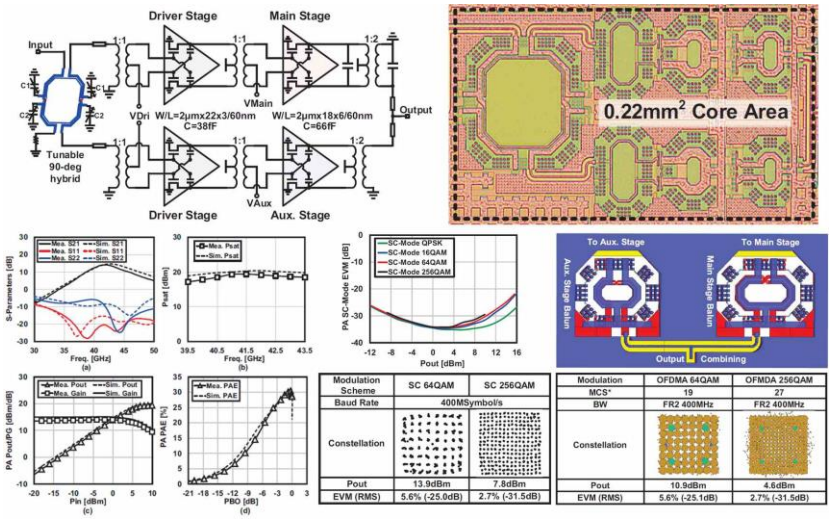

Fig. 3 Proposed Doherty PA and measurement results. **[成果 3]**

In this work, a 41-GHz CMOS transformer-based parallel-combined Doherty power amplifier is introduced. The block diagram of the 41-GHz PA is shown in Fig. 1. The amplifier consists of a tunable 90-deg hybrid and two symmetric amplifier paths. The tunable 90-deg hybrid is implemented for in-phase output combining. Each path is composed of a driver stage and an amplifier stage, both realized by differential capacitive-neutralized common-source pair. The capacitive neutralized technique is capable of enhancing the maximum available gain and reducing the Miller effect of the differential pair. The driver stages are biased at class-B for a better linearity feature. In order to conduct the load modulation, the amplifier stages of the main path and the auxiliary path are biased in class-A mode and class-C mode, respectively.

A tunable 90-deg hybrid coupler as shown in Fig. 3 is also designed to compensate the output power combining phase mismatch. Both Psat and PAE performance can therefore be compensated. Differ from the conventional 90-deg hybrid, the tunable 90-deg hybrid has three coupled line sections with the fixed characteristic impedance of $Z0$, $Z1$ and $Z0$, respectively. Two pairs of varactors are connected in shunt with the center coupled line section. When the control biases of the varactor pairs are set to 0, i.e. $VC1 = 0$ and $VC2 = 0$, the capacitance $C0$ of the varactors is obtained to perform an equivalent characteristic impedance $Z0$ together with the center coupled line section. In this case, the phase difference between $\angle S41$ and $\angle S21$ is 90°.

The proposed PA is manufactured in standard 65-nm CMOS technology. The total core chip area is 0.22mm^2. As also summarized in Fig. 3, the peak gain is 14.1dB at 41.5GHz with a −3-dB bandwidth from 39GHz to

45GHz. The measured in-band Psat is higher than 17.2-dBm with less than 2.2-dB variation. At 41.5GHz, the proposed PA achieves a 19.4-dBm Psat and an 18.6-dBm OP1dB. The peak PAE reaches 30.4% and the PAE at OP1dB is 30.1%. When operating in the deep PBO region, this PA still obtains a PAE of 19.2% at 6-dB PBO and 13.7% PAE at 8-dB PBO, respectively. To evaluate the communication capability of the proposed PA, the modulated signal measurements are performed. Under 400-MSymbols/s 64-QAM and 256-QAM modulation schemes in single-carrier mode, this work can obtain a 13.9-dBm average Pout with −25.0-dB EVM and a 7.8-dBm average Pout with −31.5-dB EVM, respectively. To demonstrate the support of the 5G NR applications, this work is also measured under 5G standard-compliant OFDMA-mode modulated signals. An average Pout of 10.9dBm in 400-MHz 64QAM is realized with –25.1-dB EVM.A 4.6-dBm average Pout in 400-MHz 256QAM is also obtained with –31.5-dB EVM.

[成果 4]

The phase and magnitude alignment between different distributed phased-array transceivers is significant. Therefore, we proposed an on-chip calibration system for aligning the phase and magnitude between different channels. Such system can be further extended between different distributed phased-arrays with proper control protocols.

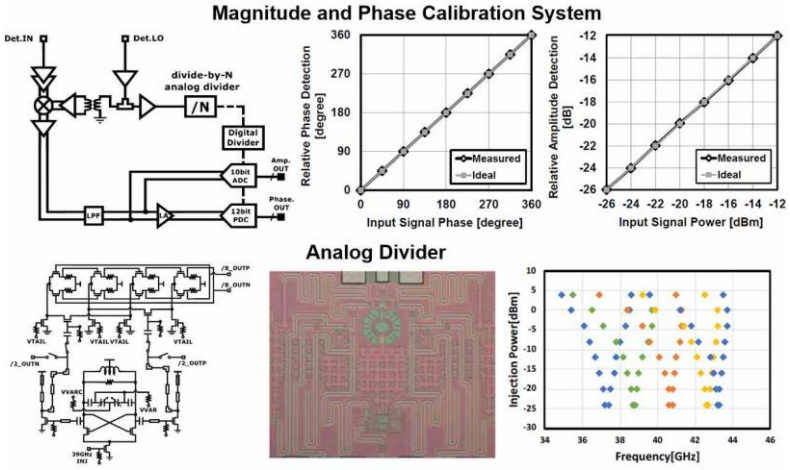

Fig. 4 Proposed Doherty PA and measurement results. **[成果 4]**

Fig. 4 shows the detail of the proposed phase and amplitude detection circuit for phased-array calibration. In Fig. 4, the block diagram of the magnitude and phase calibration block is shown. The output of the phased-array transceiver will be sent to the Det. in port of the calibration block with a frequency of 39GHz+150kHz. Then, the phase and amplitude of the transceiver output signal could be relatively detected by the proposed detection circuit. Finally, the mismatch calibration of transceiver channel could be performed by tuning the VGA and phase shifter, based on the detected digital values. Similarly, the other elements could also be calibrated in the calibration mode. In the proposed detection circuit, 39GHz-to-150kHz down-conversion scheme is utilized. The 39GHz+150kHz signal is down-converted to a detection signal around 150kHz by mixing with a 39GHz LO signal input from Det. LO port. The 150kHz detection signal is then sent to the ADC and limiting amplifier (LA) - PDC chain. With a low-frequency detection signal, high-accuracy detections with 12bits PDC and 10bits ADC are achieved easily.

Furthermore, the clock signal for PDC/ADC is generated from the detection LO. The additional reference input port can be removed for a compact system size. The on-chip clock signal generation scheme is also presented. To generate the clock signal, a frequency-divider-chain circuit is utilized. The divider chain consists of a divide-by-8 digital frequency divider, a divide-by-2 LC-type injection-locked frequency divider (ILFD) and a divide-by-4 Ring-type ILFD. Usually, the digital divider can only be used at a few GHz frequency division. However, at a much higher frequency such as 39GHz, the ILFDs are usually applied. To divide the 39GHz LO signal, a divide-by-2 LC ILFD is first utilized for low phase-noise characteristic. The conventional ILFD cannot cover enough locking range due to the degradation of injection signal at high frequency. As a result, operating frequency band of the detection circuit becomes narrow.

The magnitude of the down-converted 150KHz signal is detected by a 10-bit SAR ADC and the phase is detected by a counter-based PDC. Fig. 4 also shows the measurement results of the phase and amplitude detection accuracy of the proposed calibration system at 39GHz. The phase detection is performed from 0 degree to 360 degree, and amplitude is from -26 to -12 dBm. The measured detection results realize high-accuracy phase and amplitude detection with the PDC/ADC detection technique. The measured phase and amplitude detection errors at 39GHz are less than 0.067 degree and 0.060 dB, respectively, and the RMS detection errors are 0.049 degree and 0.036 dB, respectively. In addition, the wide-band high-accuracy detection within 37-43.5GHz is achieved. The RMS phase detection error is less than 0.060 degree, and the RMS amplitude detection error is less than 0.051 dB, respectively.

５．主な発表論文等

〔雑誌論文〕　計1件（うち査読付論文　1件／うち国際共著　0件／うちオープンアクセス　0件）

１．著者名 Li Zheng、Chen Zixin、Wang Qiaoyu、Liu Junqing、Pang Jian、Shirane Atsushi、Okada Kenichi	４．巻 20
２．論文標題 A 41-GHz 19.4-dBm Psat CMOS Doherty power amplifier for 5G NR applications	５．発行年 2023年
３．雑誌名 IEICE Electronics Express	６．最初と最後の頁 1～6
掲載論文のDOI（デジタルオブジェクト識別子） 10.1587/elex.20.20220558	査読の有無 有
オープンアクセス オープンアクセスではない、又はオープンアクセスが困難	国際共著 －

〔学会発表〕　計3件（うち招待講演　0件／うち国際学会　1件）

１．発表者名 Yi Zhang, Jian Pang, Zheng Li, Atsushi Shirane, Kenichi Okada
２．発表標題 A 39GHz Bi-direction Phased-Array Transceiver with Temperature Compensation
３．学会等名 2021 IEICE society conference
４．発表年 2021年

１．発表者名 Qiaoyu Wang, Zheng Li, Jian Pang, Atsushi Shirane, Kenichi Okada
２．発表標題 A 41GHz 19.4-dBm PSAT CMOS Doherty Power Amplifier for 5G NR Applications
３．学会等名 2021 IEICE society conference
４．発表年 2021年

１．発表者名 Yudai Yamazaki, Joshua Alvin, Jian Pang, Atsushi Shirane, Kenichi Okada
２．発表標題 A 39GHz Divide-by-8 LC-Ring ILFD Designed for 5G New Radio n260 Band
３．学会等名 2022 IEEE International Conference on Integrated Circuit Technologies and Applications（国際学会）
４．発表年 2021年

〔図書〕　計0件

〔産業財産権〕

〔その他〕

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６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考

７．科研費を使用して開催した国際研究集会

〔国際研究集会〕　計0件

８．本研究に関連して実施した国際共同研究の実施状況

共同研究相手国	相手方研究機関