【Grant-in-Aid for Scientific Research (S)】

Deep Insights into Heterointerface Engineering in Silicon Carbide based Devices

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Purpose and Background of the Research

●Outline of the Research

The electricity produced by various power plants is delivered to homes and factories. Power devices are key elements that convert and control electric power and are essential for highly efficient use of electrical energy. Silicon has been used in most conventional power devices, but they are approaching their performance limits. Power conversion with Si-based devices causes energy loss equivalent to several nuclear power plants. Therefore, improvement in efficiency and miniaturization of power devices are crucial for the wide spread of electric vehicles and their application to railroads such as the Shinkansen bullet train, as well as to various industrial devices.

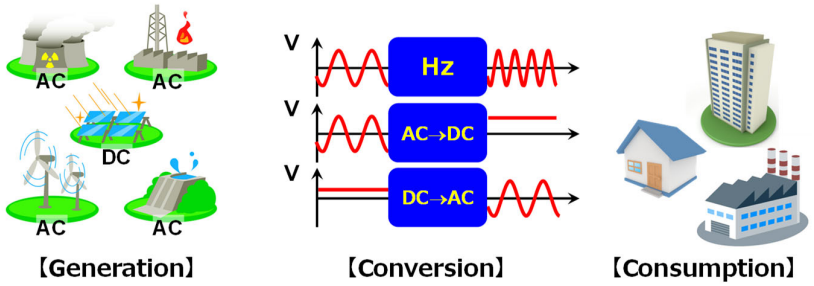

Figure 1. Flow of Electricity Generation to Consumption

Since silicon carbide (SiC) shows superior material properties, it is expected to be the suitable material for power device applications. SiC has a dielectric breakdown voltage nearly 10 times higher than that of Si and high thermal conductivity, and exhibits excellent device cooling efficiency. Although Si-based MOSFETs requires a very thick drift layer to block high voltages, SiC can reduce the thickness of the drift layer to about 1/10, which significantly reduces energy loss. In addition, the size of passive elements can also be reduced. Thus, the impact of the widespread use of SiC power devices on society is immeasurable.

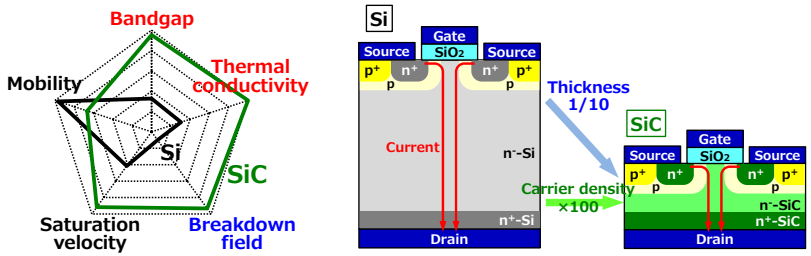

Figure 2. Material Properties of SiC and Their Advantages in Power Device Applications

●The Purpose of This Study

In MOSFETs, electrons accumulated at the MOS interface are controlled by the gate voltage. SiO_2 films formed by oxidation of SiC substrate are used as a gate insulator, but there exist many electrical defects at the SiO_2/SiC interface. The performance of SiC MOSFETs is degraded when electrons are trapped or scattered by the interface defects. In addition, change in the threshold voltage due to the carrier trapping at the interface is a major problem in terms of long-term reliability.

The origin of interface defects has been pointed out as carbon impurities generated at the SiO_2/SiC interface during SiC oxidation, but the electron capture and scattering phenomena at the MOS interface have not yet been fully explained. This study aims to deepen the basic science of SiC heterointerface and to develop a novel method for achieving an ideal SiC MOS interface.

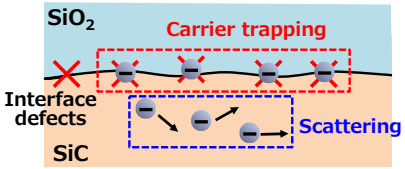

Figure 3. Issues in SiC MOS Interfaces

Expected Research Achievements

●Methods of the Research and Organization

We investigate SiC MOS interface and develop advanced method for fabricating high-quality MOS structure. To clarify the physical origins of SiC MOS interface defects, we conduct physical analyses together with theoretical study. Through first-principles calculations, we discuss possible defect structures, as well as optical properties of the system. We also conduct electrical measurements of SiC MOS devices including low-temperature measurements. To understand carrier trapping and scattering mechanisms, we fabricate dedicated SiC MOS devices and investigate their operation.

We also develop a novel method for fabricating high-quality SiC MOS structures on the basis of the above-mentioned basic research on the MOS interface. Since carbon-related defects are inevitable at the SiO_2/SiC interface formed by oxidation of SiC substrate, we develop a new process that does not involve SiC oxidation in the fabrication of MOS devices. Specifically, an ideal MOS structure is formed by depositing or bonding a high-quality insulating film under conditions that do not involve oxidation. In addition, the SiC surface is stabilized by means of plasma treatments prior to the deposition of gate dielectrics.

This research project is conducted in collaboration with Osaka University and the National Institute of Advanced Industrial Science and Technology (AIST). Osaka University has state-of-the-art clean room facilities and conduct theoretical research in addition to physical analyses and electrical measurements. AIST can conduct all processes from SiC wafer processing to device fabrication, and both institutes have a long and successful history of collaboration through MEXT programs.

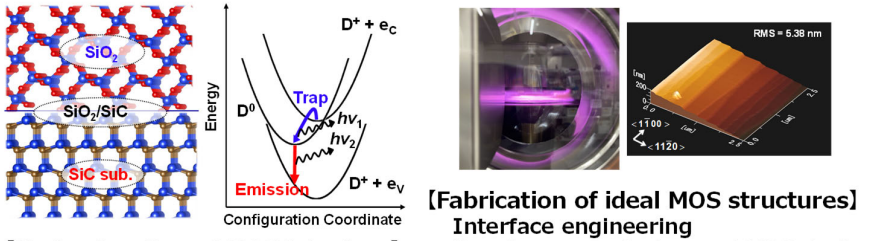

Figure 4. Schematics of the items to be implemented in this study

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