【Grant-in-Aid for Scientific Research (S)】

Integration of 2 dimensional tunnel FET for ultra-low power consumption system

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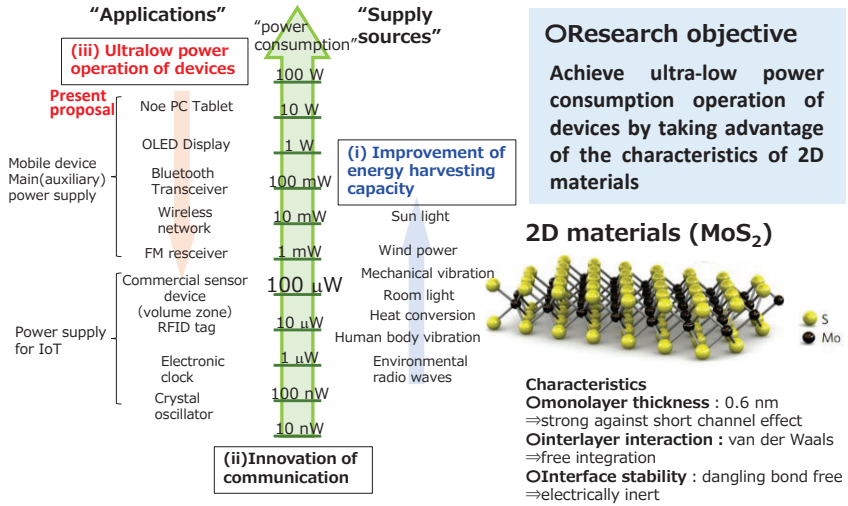
Project Information	Project Number : 22H04957　　Project Period (FY) : 2022-2026 Keywords : 2 dimensional semiconductors, Heterointerface, Tunnel effect

Purpose and Background of the Research

●Outline of the Research

Due to the influence of the new coronavirus infection, not only the digital transformation of the social infrastructure but also the lifestyle of individuals is changing. Although the number of IoT devices is expected to increase explosively, low power consumption is an essential bottleneck (Fig. 1). In this study, we demonstrate ultra-low power consumption operation by using two-dimensional materials based on "integrable" realistic device structures. In this way, we would like to contribute to the realization of ultra-low power consumption devices, which have not been achieved despite their importance.



OResearch objective

Achieve ultra-low power consumption operation of devices by taking advantage of the characteristics of 2D materials

2D materials (MoS_2)

Characteristics
Omonolayer thickness : 0.6 nm
⇒strong against short channel effect
Ointerlayer interaction : van der Waals
⇒free integration
OInterface stability : dangling bond free
⇒electrically inert

Figure 1. (Left) Three types of methods that contribute to power consumption are shown. (Right) Atomic model and features of 2D material.

●Proposal based on 2D materials

In this study, we propose for the first time a two-dimensional-tunnel field effect transistor (FET) based on an "integrable" realistic device structure. The points are (1) a simple device structure that does not use a complicated two-dimensional heterostructure, and (2) the use of Si integration process. As a result of the studies so far, as shown in Fig. 2, we found the validity of the device structure using the same in-plane junction instead of the two-dimensional heterostructures. In this study, we integrate two-dimensional-tunnel FETs using the same in-plane junction and demonstrate ultra-low power consumption operation.

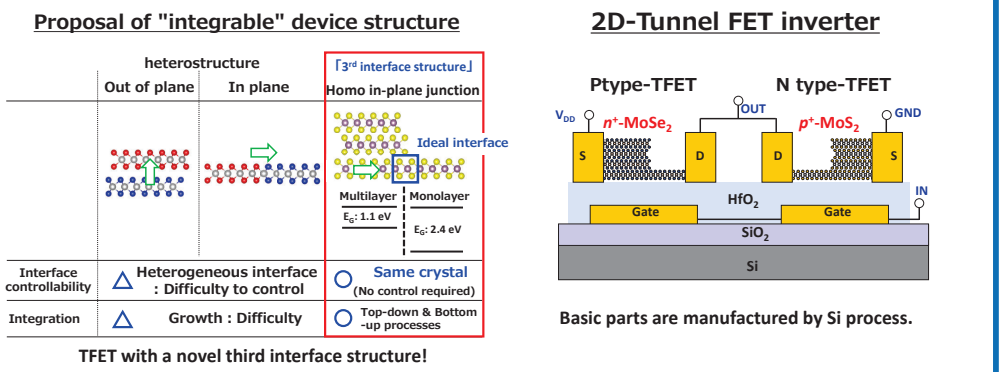


Figure 2. (Left) Three types of interface structures. (Right) Inverter based on 2D-tunnel FET.

Expected Research Achievements

●Members

As shown in Fig. 3, we collaborate with Ueno G @ Saitama University and Miyata G @ Tokyo Metropolitan University, who are leading the substitutional doping research in bulk crystal growth and large area growth.

●Achievements

The ultra-low power consumption devices require steepness of the transfer curve and high on-current in electronic devices. The following items were set to achieve the target values shown in Fig. 3. (i) Fabrication of the same crystal in-plane junction by atomic layer etching, (ii) Large area/position-controlled growth of highly doped 2D crystal, (iii) Formation of new high concentration n^+ doped 2D crystal source, (iv) Ohmic electrode formation, (v) Fabrication and evaluation of tunnel FETs. We achieve the target value and contribute to ultra-low power consumption devices.

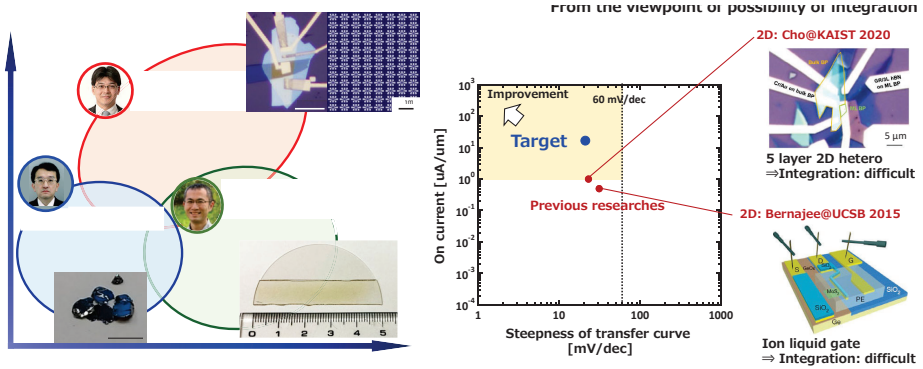


Figure 2. (Left) Members. (Right) Target & world research trends.

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