


Extension and Development of Brainmorphic Computing Principle and Hardware

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	Project Information	Project Number : 25H00447 Project Period (FY) : 2025-2029 Keywords : Brain-type computer, Brainmorphic, Brain-type Information Processing, Highly-efficient and high-performance AI hardware

Purpose and Background of the Research

●Outline of the Research

AI based on artificial neural networks (NNs) such as deep learning, and generative AI such as Chat GTP based on probabilistic statistical computation have rapidly advanced recently. However, they are causing serious social problems such as enormous power consumption. The information processing style of these AIs is very different from that of the brain in terms of highly efficient, soft, human-like information processing that the brain has acquired over many years of evolution. Therefore, a major shift in the computational paradigm is essential. To this end, we have proposed the concept of “Brainmorphic Computing Hardware” (BMCHW) as a framework for a new brain-like computing engineering system (Grant-in-Aid for Scientific Research (A) 20H00596, “Fundamentals and developments of brainmorphic computing hardware”).

In this study, we will significantly expand and develop the framework of BMCHW to a practical level. To this end, we will take a constructive approach which cycles between top-down theoretical studies and bottom-up hardware implementation. A nested complex spatiotemporal structure of the brain is reproduced as an event-driven continuous-time and continuous-value spiking NN hardware (HW) using a novel three terminal spin-orbit torque (3T-SOT) device and state-of-the-art CMOS integrated circuits. Furthermore, we will take on the challenge of elucidating the principles of brain computation through the constructive research of BMCHW. (Fig. 1)

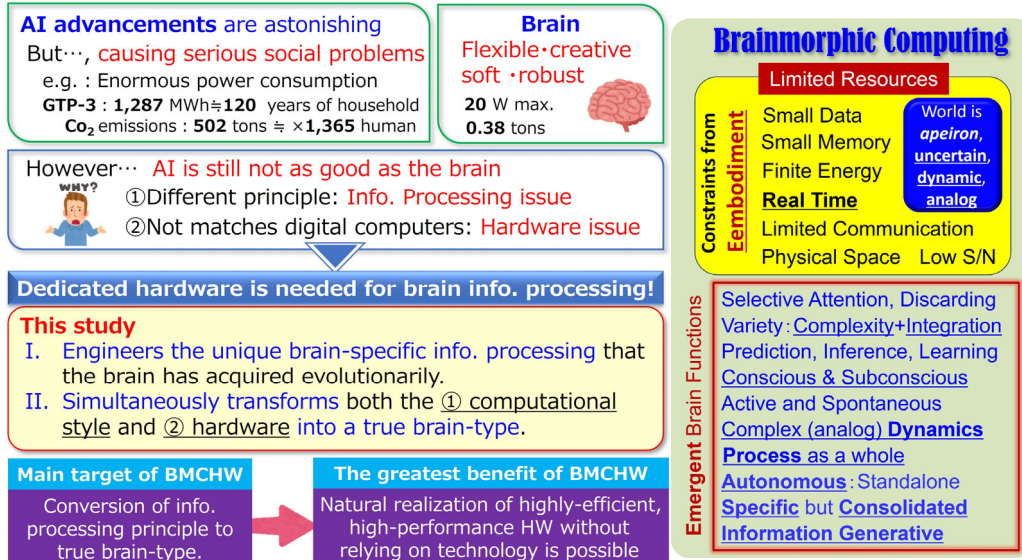
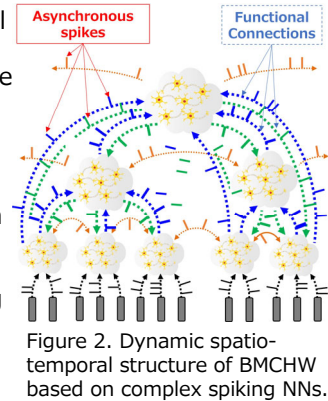


Figure 1. Aim of BMCHW research, and brain-specific information processing style to be realized.

●Research Purpose

- (1) Further develop and deepen the theory and fundamental technology of BMCHW, and bring it to the practical application level. To this end, (A) multi-time constants are introduced in addition to the multi-scale, multi-layer, multi-feedback basic structure of BMCHW using spatiotemporal asynchronous spikes (Fig. 2), and (B) event-driven, asynchronous, continuous-time/value spiking NN HW is developed using brain-like devices such as the 3T-SOT device.
- (2) We take a constructive strategy that involves repeatedly verifying and updating working hypotheses by comparing the behavior of the hardware with mathematical models and physiological experiments, to elucidate the principle of information processing in the brain.



Expected Research Achievements

●Three levels of theoretical and practical researches

[WP1] “Brain component level”:

(A) Realize ultra-low power modified Izhikevich neuron CMOS integrated circuit that generates a variety of spiking patterns. (B) Implement spike timing-dependent plasticity and spatiotemporal learning rules using analog nonvolatile 3T-SOT devices.

[WP2] “Element network level”:

(A) Develop efficient spatiotemporal information representations using various spiking patterns such as chaotic spike sequences for fractal coding. (B) Develop theories and implementations of spatiotemporal contextual learning memory NNs. (C) Implement complementary recognition systems with vision and hearing using multi-modal reservoir NNs and predictive coding through reservoir NNs.

[WP3] “Global Network Level”:

(A) Construct a conscious/subconscious hybrid computing HW system based on quick dynamical switching between high-dimensional attractors. (B) Develop a global instantaneous control method that instantly switches between processing modes.

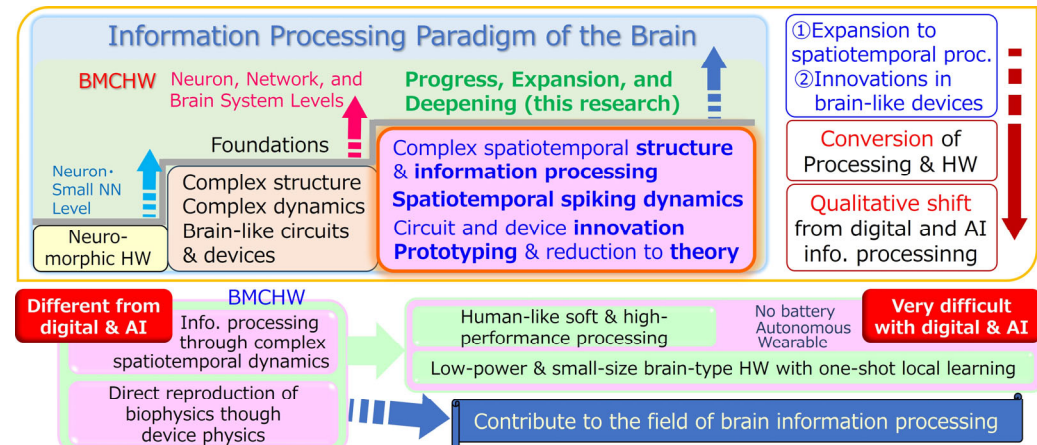


Figure 3. Research content, ripple effects, and contributions to academia. The BMCHW platform will be significantly developed through constructive research of processing principle and hardware.