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研究課題名（和文）Fabrication of high current output fin-type diamond field-effect transistors

研究課題名（英文）Fabrication of high current output fin-type diamond field-effect transistors

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交付決定額（研究期間全体）：（直接経費）　　3,200,000円

研究成果の概要（和文）：大面積の単結晶ダイヤモンドウェーハ不足の為に、ダイヤモンド電子デバイスのダウンスケーリングに必要がある。本研究では、水素終端ダイヤモンドトリプルゲート金属-酸化物-半導体電界効果トランジスタ(MOSFET)を開発した。デバイスの電気的特性は、同一基板上に同時に製造されるプレーナ型MOSFETと比較される。トリプルゲートMOSFETの出力電流は、プレーナ型デバイスよりはるかに高く、オン/オフ比とサブスレッショルドスイングは10e8以上と110mV/decである。これらのダイヤモンドトリプルゲート電界効果トランジスタは、ダイヤモンド電子デバイスを実際応用に向けて推進することがある。

研究成果の概要（英文）：Excellent physical properties of semiconductor diamond make it a promising candidate for high-power and high-frequency electronic device. However, lack of large-area single-crystal diamond wafers hinders electronic devices for practical applications. This issue leads us to downscale diamond electronic devices. Triple-gate metal-oxide-semiconductor field-effect transistor (MOSFET) architecture offers a way to extend device downscaling and increase device output current. Here, we design and fabricate a hydrogenated diamond (H-diamond) triple-gate MOSFET. The triple-gate MOSFET’s output current is much higher than that of the planar-type device, and the on/off ratio and subthreshold swing are more than 10e8 and as low as 110 mV/dec, respectively. The fabrication of these H-diamond triple-gate MOSFETs will drive diamond electronic device development forward towards practical applications.

研究分野：電子デバイス・電子機器

キーワード：ダイヤモンド　電界効果トランジスタ　MOSFET

１．研究開始当初の背景

It is well-known that wide bandgap semiconductors such as GaN, SiC, and diamond are suitable to replace silicon partly for fabrication of high-power and high-frequency electronic devices because of their large band-gap energies, high carrier mobility, and high breakdown field. According to figure of merit, diamond-based electronic devices have the largest power-frequency product, the highest thermal limitation, and the lowest power-loss at high frequency. Therefore, it is promising to fabricate high-performance diamond electronic devices for practical applications. Recently, fabrication of diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) has been developed greatly. Most of them have been fabricated on hydrogenated-diamond (H-diamond) epitaxial layers. In our previous studies, planar-type and T-type H-diamond MOSFETs have been fabricated successfully. However, it is difficult to further increase its current output. Since the triple-gate fin-type diamond MOSFET is believed to generate several times higher current output than that of planar-type or T-type one. We propose to fabricate it in this project.

２．研究の目的

In this project, we propose to fabricate a novel triple-gate fin-type H-diamond MOSFET. The current output of it is considered to be several times higher than those of the planar-type and T-type one. Additionally, the triple-gate fin-type H-diamond MOSFET has the other advantage of the device size scaling. The fabrication of small size high current output triple-gate fin-type H-diamond MOSFET will possibly push forward the diamond electronic devices for the practical application.

３．研究の方法

(1) The fin-pattern diamond was formed using an inductively-coupled plasma reactive ion etching (RIE) technique. The etching conditions were investigated and optimized. After forming the fin-pattern, high-quality H-diamond epitaxial layer was grown on the fin-pattern diamond by microwave plasma-enhanced chemical vapor deposition technique

(2) The H-diamond triple-gate MOSFET was fabricated based on a combination of electron beam lithography, capacitively-coupled plasma RIE dry-etching, electron gun evaporation, atomic layer deposition, sputtering, wet etching, and lift-off techniques.

(3) The surface morphology of the fin-pattern diamond substrate was investigated using scanning electron microscopy (SEM) system. Transmission electron microscopy (TEM) measurements were performed using the JEM-2100F system with an accelerating voltage of 200 kV. Electrical properties of the MOSFETs were measured using an MX-200/B prober and a B1500A parameter analyser (Agilent, Tokyo, Japan).

４．研究成果

(1) Surface and interface morphologies

Figure 1 shows SEM [Figs. 1(a), 1(b), and 1(c)] images of the fin-patterned diamond substrate and triple-gate MOSFET, and TEM [Figs. 1(d), 1(e), 1(f), and 1(g)] images of interface of the triple-gate H-diamond MOSFET. The total width of the diamond fin pattern and the fin length are 100.5 and 7 μm, respectively. Both the fin width and the interspacing between fins are 500 nm. The fin height was confirmed using a 3D-measurement laser microscope to be 500 nm. Obvious gate, source, and drain contacts for the H-diamond triple-gate MOSFET can be observed in Fig. 1(c). After H-diamond epitaxial layer growth by the MPCVD technique, the fin length and width increased to 7.8 μm and 600 nm, respectively. The interspacing between fins and the fin height both decreased to 400 and 340 nm, respectively [Fig. 1(d)]. The H-diamond epitaxial layer thickness is approximately 50 nm [Fig. 1(e)]. Fig. 1(f) shows a high-resolution TEM image for the zoom of the left adjacent fins in the Fig. 1 (d). The angle between two adjacent fins is 60°. The equivalent gate width (W_G) for the triple-gate MOSFET can be calculated to be 139.6 μm. The ALD-Al_2O_3 layer thickness is approximately 27.9 nm, which is in good agreement with the measurement results obtained using an ellipsometer system. An interfacial layer with thickness of around 0.6 nm exists between H-diamond and Al_2O_3 [Fig. 1(g)].

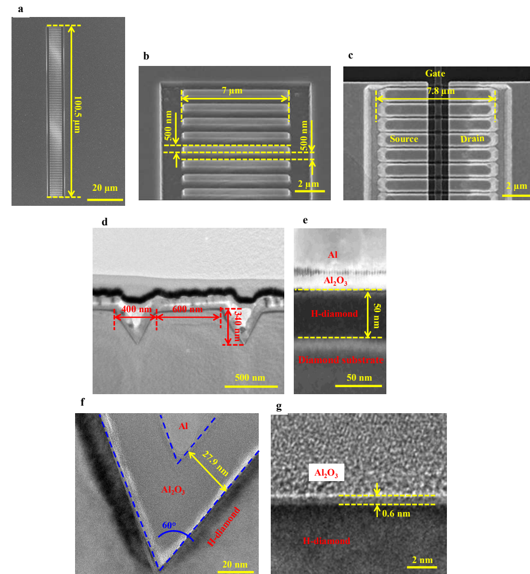

Figure 1. (a) and (b) SEM images of the fin-patterned diamond substrate. (c) SEM image of the triple-gate MOSFET. (d), (e), (f), and (g) Interfacial TEM images of the triple-gate H-diamond MOSFET.

(2) Electrical properties of triple-gate and planar-type MOSFETs

Figure 2 shows (a) and (b) drain-source current versus voltage (I_{DS}-V_{DS}) characteristics for

the triple-gate and planar-type MOSFETs, respectively. The V_{GS} is varied from −10.0 to 20.0 V in steps of +1.0 V. The I_{DS} for the planar-type MOSFET was normalized with the W_G of 100.5 μm. That for the triple-gate MOSFET was normalized with its equivalent W_G of 139.6 μm. Both MOSFETs show obvious *p*-type channel and pinch-off characteristics. There are also good linear relationships between I_{DS} and low V_{DS} for both devices. The absolute drain-source maximum ($I_{DS,max}$) for the triple-gate MOSFET is 174.2 mA mm^{-1}, which is much higher than the value of 45.2 mA mm^{-1} obtained for the planar-type device. The value of on-resistance (R_{ON}) can be extracted from the linear region of the I_{DS}–V_{DS} characteristics, and is 31.9 and 98.0 Ω mm for the triple-gate and planar-type MOSFETs, respectively. The R_{ON} for the triple-gate H-diamond MOSFET is composed of the fin pattern channel resistance beneath the Al_2O_3 insulator (R_{CH}), the fin pattern H-diamond surface resistance with the $L_{S/D\text{-}G}$ of 500 nm ($2R_{SD}$), and the ohmic contact resistance ($2R_C$). Because $2R_C$ is much smaller than R_{CH} and $2R_{SD}$, it can be neglected here. By combining the R_{ON} value of another two triple-gate MOSFETs with the $L_{S/D\text{-}G}$ of 1.0 and 2.0 μm, R_{CH} and $2R_{SD}$ for the triple-gate MOSFET can be deduced to be 23.8 and 8.1 Ω mm, respectively.

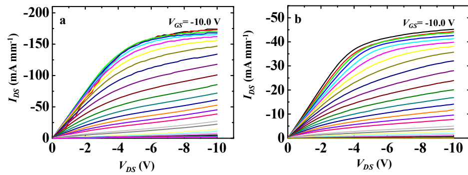

Figure 2. (a) and (b) I_{DS}-V_{DS} characteristics for the triple-gate and planar-type MOSFETs, respectively. The V_{GS} is varied from –10.0 to 20.0 V in steps of +1.0 V.

(3) Transfer characteristics for triple-gate and planar-type MOSFETs.

The transfer characteristics that correspond to the I_{DS}–V_{DS} curves are shown in Fig. 3. The on/off ratio of the triple-gate MOSFET is higher than 10^8 [Fig. 3(a)], and is the same level as that of the planar-type device [Fig. 3(d)]. The SS is an important parameter for evaluation of MOSFET power consumption, and is defined as the inverse slope of log $|I_{DS}|$ versus V_{GS}. The sub-threshold swing (SS) is 110 mV dec^{-1} for the triple-gate MOSFET at a V_{DS} of −10.0 V [Fig. 3(a)]. This value is much lower than that of the planar-type device of 460 mV dec^{-1} [Fig. 3(d)]. The threshold voltage (V_{TH}) values of the MOSFETs can be determined based on $-\sqrt{|I_{DS}|}$ as functions of V_{GS}, and are 10.2±0.1 and 7.6±0.1 V for the triple-gate and planar-type MOSFETs, respectively [Figs. 3(b) and 3(e)]. The extrinsic transconductance (g_m) is determined based on the slope of the I_{DS}–V_{GS} curve. The maximum g_m values for the triple-gate and planar-type MOSFETs are 15.3±0.1 and 3.8±0.1 mS mm^{-1}, respectively [Figs. 3(c) and 3(f)].

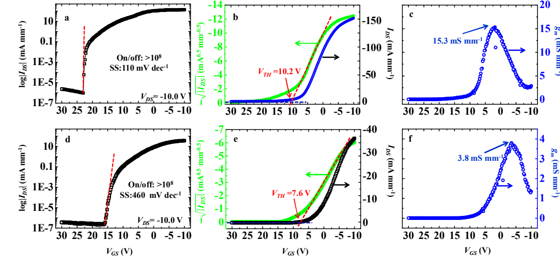

Figure 3. (a), (b), (c) The log $|I_{DS}|$–V_{GS}, $-\sqrt{|I_{DS}|}$–V_{GS}, and g_m–V_{GS} characteristics of the triple-gate MOSFET, respectively. (d), (e), (f) The log $|I_{DS}|$–V_{GS}, $-\sqrt{|I_{DS}|}$ –V_{GS}, and g_m–V_{GS} characteristics of the planar-type MOSFET, respectively.

５．主な発表論文等

（研究代表者、研究分担者及び連携研究者には下線）

〔雑誌論文〕（計　7　件）

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DOI: 10.1063/1.5022590

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⑦ F.N. Li, J.W. Liu, J.W. Zhang, X.L. Wang, W. Wang, Z.C. Liu, H.X. Wang, Measurement of barrier height of Pd on diamond (100) surface by X-ray photoelectron spectroscopy, Applied Surface Science, Reference reading, 370, 2016, 496-500.
DOI: 10.1016/j.apsusc.2016.02.189

〔学会発表〕（計　20　件）

(1) Invited talk

① J. W. Liu, “Diamond NOT and NOR logic circuits composed of enhancement-mode and depletion-mode MOSFETs”, 2017 Cross–Strait Seminar on Diamond Films and Functional Devices, Taiwan, 2017.10.26-10.29.

② J. W. Liu, “Semiconductor diamond-based MOS electronic devices”, 4th Annual Global Congress of Knowledge Economy-2017, Qingdao, China, 2017.9.19-9.21.

③ Y. Koide, J. W. Liu, M. Imura, M. Y. Liao, “Normally-on/off control of diamond FETs and logic circuit demonstration”, The 2017 E-MRS Fall Meeting and Exhibit, Warsaw, Poland, 2017.9.18-9.21.

④ J. W. Liu, “Diamond field-effect transistors”, 3rd Annual International Workshop on Materials Science and Engineering, Guangzhou, China, 2017.9.8-9.10.

⑤ J. W. Liu, “Recent development for semiconductor diamond based MOSFETs”, The Int'l Conference on New Materials and Applications（NMA 2017), Guilin, China, 2017.7.20-7.22.

⑥ J. W. Liu, “Recent developments for our diamond electronic device”, 2017 Collaborative Conference on Materials Research (CCMR), Jeju Island, Korea, 2017.6.26-6.30.

⑦ J. W. Liu, “Single crystalline diamond MOSFETs and logic circuits”, 2016 China International Carbon Materials Conference, Shanghai, China, 2016.12.8-12.9.

⑧ J. W. Liu, “Hydrogenated diamond MOSFETs and logic circuits”, Nanotechnology-2016, Singapore, 2016.11.7-11.9, oral.

⑨ J. W. Liu, “Our Recent Studies on Diamond Electronic Devices”, University of Science and Technology Beijing visiting, Beijing, China, 2016.4.25-4.26.

⑩ J. W. Liu, “Semiconductor diamond metal-insulator-semiconductor field-effect transistors”, EMN East Meeting 2016, Beijing, China, 2016.4.22-4.25.

(2) International conference

① J. W. Liu, M. Y. Liao, M. Imura, and Y. Koide, “Logic circuits with hydrogenated diamond MOSFETs”, 2017 International Conference on Diamond and Carbon Materials, Gothenburg, Sweden, 2017.9.3-2017.9.7, poster, general.

② J. W. Liu, H. Oosato, X. Wang, M. Y. Liao, Y. Koide, “Fabrication of triple-gate hydrogenated diamond MOSFETs” 2017 International Conference on Diamond and Carbon Materials, Gothenburg, Sweden, 2017.9.3-2017.9.7, poster, general.

③ J. W. Liu, H. Oosato, M. Y. Liao, M. Imura, E. Watanabe, Y. Koide, Diamond logic circuits with depletion- and enhancement-mode MOSFETs. 29th International Conference on Defects in Semiconductors, Matsue, Japan, 2017.7.31-8.4, poster, general.

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⑥ J. W. Liu, M. Y. Liao, M. Imura, B. Ryan, and Y. Koide, “High-*k* TiO_2 on diamond for electronic devices: capacitor, field-effect transistor, and logic inverter” 10th International Conference on New Diamond and Nano Carbons, Xi’an, China, 2016.5.22-5.26, oral, general.

(3) Domestic conference

① J. W. Liu and Y. Koide, ダイヤモンド論理回路チップの開発, SATテクノロジーショーケース2018, 2018.2.8

② J. W. Liu, M. Y. Liao, M. Imura, and Y. Koide, “Diamond NOT and NOR logic circuits”, The 64th JSAP Spring Meeting, Yokohama, Japan, 2017.3.14-3.17, poster, general.

③ J. W. Liu, M. Y. Liao, M. Imura, B. Ryan, and Y. Koide, “Fabrication of hydrogenated diamond logic circuits”, The 30th Diamond Symposium, Tokyo, Japan, 2016.11.14-11.16, oral, general.

④ J. W. Liu, H. Oosato, X. Wang, M. Y. Liao, Y. Koide, “Fabrication of triple-gate fin-type hydrogenated diamond MOSFETs”, The 77th JSAP Autumn Meeting, Niigata, Japan, 2016.09.13-09.16, oral, general.

〔図書〕（計　1　件）

① J. W. Liu and Y. Koide, “Fabrication of hydrogenated diamond metal-insulator-semiconductor field-effect transistor”, Biosensors and Biodetection, Chapter 15, Springer, 217-232 (2017).

〔産業財産権〕

○出願状況（計　2　件）

(1)
名称：トリプルゲートＨ－ダイヤモンドMISFET及びその製造方法
発明者：J. W. Liu, Y. Koide, H. Oosato, X. Wang, M. Y. Liao
権利者：国立研究開発法人物質・材料研究機構
種類：特許
番号：特願 2016–112611
出願年月日：2016.06.06
国内外の別：　国内

(2)
名称：ダイヤモンド半導体装置、それを用いたロジック装置、及びダイヤモンド半導体装置の製造方法
発明者：J. W. Liu, Y. Koide, H. Oosato, M. Y. Liao, M. Imura
権利者：国立研究開発法人物質・材料研究機構
種類：特許
番号：特願 2016-220840
出願年月日：2016.11.11
国内外の別：　国内

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