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研究課題名(英文)A Concept-proof Study of Multibeam Heterodyne Receiver Frontends for Next Generation Radio Telescopes
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研究成果の概要(和文):本研究は小型超伝導マルチビーム受信機を構築する技術にブレークスルーをもたらす ことを目的とする。主な成果は以下の通りである。(1)ハイブリッド平面集積法(HPI)を提案した。この手法に は2つの要素があり、シリコンベースの超伝導モノリシックマイクロ波集積回路(MMIC)製造技術と2D金属導波 管L0分配ネットワークに関連するシリコンメンブレンベースの導波管プローブである。(2)125-164GHz帯におい てHPIを用いて概念実証のための単一ピクセル受信機を開発した。(3)HPIを用いて2×2の小型化アレイ受信機を 開発した。このアレイは従来にない小型化を実現し、良い単一ピクセル性能を示した。

研究成果の学術的意義や社会的意義 現在の電波望遠鏡の弱点の一つは、視野が狭いことである。視野の狭さは、星に進化する分子雲などの広い天体 を観測する能力を著しく低下させる。このような天体を撮影するためには、望遠鏡のビームをスキャンするため に莫大な観測時間を費やさなければならない。この問題を解決するには、望遠鏡の焦点面に複数の検出器を持つ マルチビーム受信機を使用する必要がある。しかし、電波望遠鏡用マルチビーム受信機を構築することは技術的 に難しい。本研究では、この問題に取り組み、ミリ波からテラへルツ波までの一次も現代電波 望遠鏡用のマルチビーム受信機を構築するための実現可能な解決策を提案することを目的とする。

研究成果の概要(英文):This study aims to make essential breakthroughs in the techniques of constructing large-format and compact superconducting multi-beam receiver frontends. The major achievements are as follows. (1) An innovative approach, hybrid planar integration (HPI), has been proposed and developed. This approach has two components. One is silicon-based superconducting monolithic microwave integrated circuit (MMIC) fabrication technique; The other is silicon membrane-based waveguide probes and associated two-dimensional metal waveguide LO distributing network. (2) A single-pixel proof-of-concept receiver based on HPI approach has been developed at 125-164 GHz frequency band. The measurement results approach state-of-the-art performance;(3) A 2 x 2 compact array receiver has been developed at the same frequency band by implementing HPI approach. This array achieved the unprecedent compactness and demonstrated even LO distribution and unaffected single-pixel performance.

研究分野: 電波天文用受信機の開発

キーワード: multibeam receiver radio astronomy SIS mixer HPI MMIC

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1. 研究開始当初の背景

The narrow field-of-view (FOV) for modern-day radio telescope is a significant limitation for surveys requiring large area mapping, such as galactic star formation regions, nearby galaxies, Magellanic Cloud studies, and solar observations, which are usually diffused. For distant universe observations, even though the objects are not resolved, statics of gas in high-z galaxies suffers a lot by low efficiency. Wide FOV will also be important in terms of synergetic studies with future instruments such as TMT. Broadening of FOV of radio telescopes by using large-format focal plane array is recognized as important task in present technical development.

While direct detection cameras with thousands of pixels have been developed, large-format multipixel heterodyne receivers are completely absent because of enormous technical difficulties. On the other hand, the focal plane of nextgeneration telescopes will allow thousands of pixels. Therefore, the key question presented to us is what new multibeam frontend technology can be worked out to make better use of the focal plane.

2. 研究の目的

Our aim is to make essential technical breakthroughs in the multibeam receiver integration. The new techniques will lead to new type of instrument, which allow us to realize frontends (1) with pixel number 100~1000, dramatically broadening the FOV of single dish telescope, and (2) with small N~10 close-packed horn array can be applied to broaden the FOV of interferometers like Atacama Large Millimeter/Submillimeter Array (ALMA).

Our goal is to establish a new concept in constructing Superconductor-Insulator-Superconductor (SIS) multibeam frontends, the most sensitive mixer reaching zero-point fluctuation noise level. This approach must enable all the following advanced technical features, namely dual polarization, sideband separation (2SB) and balanced mixing, in to a compact multibeam frontend.

3. 研究の方法

The conventional approach to build a multibeam SIS receiver is assembling individual single-pixel modules. Because of the prohibitive difficulties in assembly, only very sparse array can be realized with small number of pixels. Our method, which is named hybrid planar integration (HPI), is based on an embedded LO distribution network supported by a monolithic SIS integrated circuit (MMIC). The central idea of the concept comprises two components, namely, (1) monolithic sideband-separation (or balanced) SIS mixer circuit with on-chip planar OMT, and (2) embedded waveguide LO distribution network. This approach eliminates most of the external interconnection and therefore allows highest compactness and much improved reliability.

The study largely relies on microfabrication techniques. The microfabrication is carried out in the cleanroom facility of national astronomical observatory of Japan, from which we have been producing high-quality SIS mixers for ALMA telescope. Silicon-on-insulator wafers are adopted in this study as the substrate of MMICs, which allow realizing membranes where waveguide probes locate by removing the handling wafer with deep reactive ion etching. Various methods to improve the fabrication yield of MMICs have been investigated. We have set up dedicated RF measurement setup for the assessment of the MMICs and prototype receivers. Homemade SIS mixer design software SISMA [1] and commercial EM simulator (HFSS) are used in the circuit design.

4. 研究成果

The achievement will be concluded as the following four points.

We introduced a design concept (HPI) that enables planar integration of an SIS array receiver frontend, which sets up a framework for large format arrays. This method has an exceptional merit, i.e. one can incorporate dual-polarization, balanced mixing and sideband separation into a very compact heterodyne array receiver frontend. This concept was published in [2] with title "A New Concept for Quasi-Planar Integration of Superconductor-Insulator-Superconductor Array Receiver Frontends."

By applying this concept, we developed a single-pixel prototype SIS receiver to make experimental verification. The prototype planar superconducting SIS mixer circuit operating at 2 mm with dual polarization and balanced configuration that has not been challenged in a monolithic planar circuit before. The results not only proofed the feasibility of the concept by showing correct response of the receiver, also demonstrated high quality of the performance. The receiver noise temperature is as low as about 40 K and show little frequency dependence. The noise rejection ratio (a figure-of-merit of balance circuit) is as high as 15 dB, and the cross polarization is lower than 20 dB. All these performances are comparable to the best performance that a conventional SIS mixer can reach. This means that little penalty in performance has to paid to achieve the highly compact integration in the new approach. [3, 6, 8]



Fig.1 Left: The image of the front side of the MMIC chip with a size of 13 mm \times 10 mm \times 0.4 mm. Right: the measured heterodyne mixing responses and noise temperature of the MMIC. (from [2])

4.2 Microfabrication methods that support HPI

The implementation of HPI concept relays on the establishment of dedicated fabrication process. To fabricate high quality devices various new techniques were applied in the fabrication. Four of them deserve to be emphasized. [4,5,7]

(1) silicon-on-insulator (SOI) wafers together with deep reactive ion etching are adopted for fabricating membranes that are locally formed on the silicon handling wafer. (2) Plasma-enhanced chemical vapor deposition (PECVD) is adopted rather than the more conventional magnetron sputtering for better side-wall coverage. (3) A machine-aligned via-hole etching process provides improved uniformity in the junction definition and therefore leads to good balance of the circuit. (4) We introduced a compressive/tensile/compressive SiO₂ tri-layer technique with using PECVD. Thanks to this method the device quality and yield significantly improved.



Fig.2 Photographs of (a) front side and (b) backside of the MMIC chip. SEM images of some detailed structures are shown in (c)-(e). (c) DC blockage capacitor. (d) Three SIS junctions connected in series. (e) CPW cross-over. (from [5])

4.3 Prototyping of 2 x 2 SIS mixer array

A 2 \times 2 dual-polarization balanced SIS mixer array has been developed by implementing HPI scheme and been assessed in 125-163GHz RF band. This compact array has demonstrated uniform LO distribution and low crosstalk (-30 dB) between pixels. The RF performance of component pixels has been confirmed to be little affected by the high-degree integration. This demonstration is the most important goal of this study and has been successfully accomplished. [9, 10, 11]



Fig.3 Architecture of the 2 \times 2 array frontend. On the left is the exploded views of the CAD model presented in two different perspectives. On the upper right is the front view of the mixer chip, on which there are two balanced mixers and membrane-based probes that couple LO and signal from metal waveguides. An SEM image shows the tuning circuit of the SIS mixer that consists of three tunnel junctions in series and short tuning inductive lines. (from [10])

4.4 Sideband separation MMIC mixers and related fabrication methods

We have made breakthroughs in fabrication of thin-film resistors based on nitrogendeficient NbTiN by using reactive sputtering. This achievement enabled us to proceed with the development of sideband separation (2SB) mixer MMICs. By applying the NbTiN thin-film resistor fabrication method, we have fabricated 2SB MMIC devices. Preliminary measurement results demonstrated expected sideband separation performance. This study will be continued and become a research topic in the successive KAHENHI project. Reference:

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2.発表標題

A Millimeter-wave Multibeam Receive Implemented with Superconducting MMICs

3 . 学会等名

応用物理学会秋季年会

4.発表年

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江崎翔平

2.発表標題

PE-CVDプロセスがSISミキサ集積回路に及ぼす影響

3.学会等名
 応用物理学会秋季年会

4 . 発表年

2020年

〔図書〕 計0件

〔産業財産権〕

〔その他〕

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6.研究組織

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7.科研費を使用して開催した国際研究集会

〔国際研究集会〕 計0件

8.本研究に関連して実施した国際共同研究の実施状況

	共同研究相手国	相手方研究機関			
中国		Purple Mountain Observatory			
韓国		KASI			