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研究課題名（和文）High-frequency and low power-consumption GaN monolithic complementary power integrated circuits

研究課題名（英文）High-frequency and low power-consumption GaN monolithic complementary power integrated circuits

研究代表者

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研究成果の概要（和文）：1) 二次元正孔ガスを持つInGaN/GaNヘテロ構造の開発が成功した。ヘテロ界面の急峻性、組成制御、歪みの影響なとの事項について検討した。2)InGaN/GaN pチャネルMOSFETsの開発が成功し、低温８Kまでの動作を実証した。二段階の表面処理法及びCaF2やSiNx 絶縁ゲート膜を利用したMIS界面はMOS界面より、界面準位密度と捕獲電荷は約１桁を減少した。3)MOCVDより、AlGaN/GaN-on-Siウェハの上にInGaN/GaNヘテロ構造の応力制御、格子緩和度および不純物混入に与える影響を調べした。さらに、InGaN系とAlGaN系のCMOS集積回路の設計と開発した。

研究成果の学術的意義や社会的意義
In recent years, with the power increasing of GaN electronic devices, the current Si-based integrated circuits can not meet high-power operations. Our proposed GaN-based CMOS to drive GaN electronic devices is promising and can be energy-saving, environment freely, and compact in size.

研究成果の概要（英文）：1)The two-dimensional hole gas at the InGaN/GaN was successfully achieved by experiment. The growth conditions were optimized and a super-thin GaN interlayer was utilized to improve the hole concentration. 2)The p-channel MOSFETs were successfully fabricated, which can be working at the temperature as low as 8K. The interface defects at the MOS was reduced by using the two-step treatment and oxygen-free gate dielectric layrs. 3)The InGaN/GaN p-channel heterojunction was deposited on the AlGaN/GaN HEMT wafer to fabricate the complementary power CMOS circuits. The lattice mismatch was investigated, and high-quality heterojunction was obtained. Both the n-channel and p-channel MOSFETs were fabricated. The device performance was characterized.

研究分野：半導体工学

キーワード：窒化物半導体　電界効果トランジスタ

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１．研究開始当初の背景

Recent advances in the GaN power electronics have demonstrated the superior performance including a much lower specific on-resistance, higher breakdown voltage (over 5kV), higher speed (<ns), and higher temperature (up to 1000℃) over Si electronics for high-power switching applications. ***However***, the **equally high-performance integrated circuits** with high frequency and low switch loss **to drive these power diodes or FETs** have not been exploited, which hinders the real applications of the GaN-based power electronics. The conventional Si-based power ICs are reaching their system limits and show the drawbacks of a high leakage current and poor reliability especially at harsh conditions. The GaN complementary CMOS power ICs are expected to manage electricity more efficiently while having a significantly smaller form factor, owing to their intrinsic high breakdown voltage, high carriers mobility, and superior physical and chemical stability. Nevertheless, compared to the *n*-channel AlGaN/GaN high electron mobility transistors (HEMTs), the development of *p*-channel FETs using two-dimensional hole gas (2DHG) is far from their ideality. To achieve a high-performance GaN CMOS power IC, *p*-channel FETs with effectively high hole mobility and low on-resistance which can be comparable with *n*-channel ones is in great demand.

２．研究の目的

In this proposal, we propose to fabricate the GaN-based one-chip monolithic complementary power ICs by fabricating InGaN/GaN *p*-channel MOSFETs on the AlGaN/GaN *n*-channel HEMTs. There are several advantages of this novel power CMOS ICs: 1) higher holes mobility and concentration than GaN/AlGaN *p*-channel, 2) easy integration without crack problem, 3) wide-range working temperatures,4) feasibility of normally-off operation during growth.

３．研究の方法

To achieve this aim, the following scientific problems should be solved. **Firstly**, high-mobility 2DHG should be developed at InGaN/GaN heterojunctions. This remains a difficult due to the high *n*-type background conductivity and impurity scattering at the heterointerface. **Secondly**, the integration growth of atomic-level smooth heterojunctions of InGaN/GaN on AlGaN/GaN should be performed. **Thirdly**, the normally-off operation for both *n*-channel and *p*-channel FETs should be achieved.

The research methods are as follows.

1) The high-quality InGaN/GaN heterojunctions are epitaxially grown by MOCVD and high-pressure MOCVD (HPMOCVD)
2) The p-channel MOSFETs are designed and fabricated.
3) Integrated growth of p-channel InGaN/GaN heterojunction on AlGaN/GaN structures
4) Fabrication, characterization and reliability of the GaN complementary power circuits

４．研究成果

The achievements during the two years are:

1) Successfully obtain the 2DHG at the InGaN/GaN heterojunction from experiment

Firstly, we designed the structure of the InGaN/GaN heterojunction by a simulation using self-consistent solution of Poisson-Schrödinger equations combined with polarization-induced theory. The band diagram, hole concentration, and distribution can be obtained from the simulations. As a result of piezoelectric polarization between InGaN and GaN, high-density negative polarization charges are created at the lower interface of pseudomorphic InGaN/GaN heterostructure. To compensate these fixed charges, hole accumulation with large band bending happens near the interface of InGaN/GaN heterostructure. From the simulation, the optimized thickness for the strained InGaN is 90 nm and In composition of 25%. The optimized structure was grown by using the metal organic chemical vapor deposition

(MOCVD) and high-pressure MOCVD. Before InGaN deposition, a long-time growth interrupt in both nitrogen and ammonia ambient was introduced to polish the interface, followed by a super-thin unintentionally doped GaN (UID-GaN) spacer layer with an ultra-flat morphology. The growth interrupt can improve the interface quality, which was confirmed in our previous study. Slightly Mg-doping is performed for the strained InGaN layer to compensate the n-type background concentration.

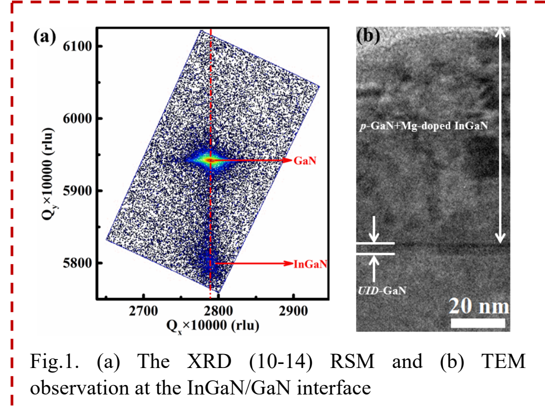
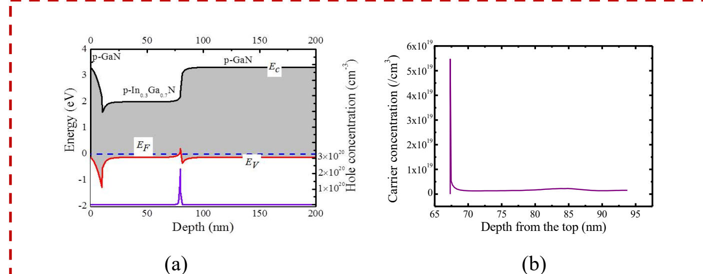


Fig.1. (a) The XRD (10-14) RSM and (b) TEM observation at the InGaN/GaN interface

The high-resolution X-ray diffraction (HRXRD) reciprocal space mapping (RSM) around (10–14)- plane reveals that the InGaN layer is totally strained on the GaN template, ensuring a good quality with large piezoelectric polarization field (Fig. 1(a)). Figure 1(b) shows the cross-sectional bright field transmission electron microscopy (TEM) image of the InGaN/GaN heterojunction. An abrupt interface can be clearly seen at the view in a high magnification.



(a) (b)

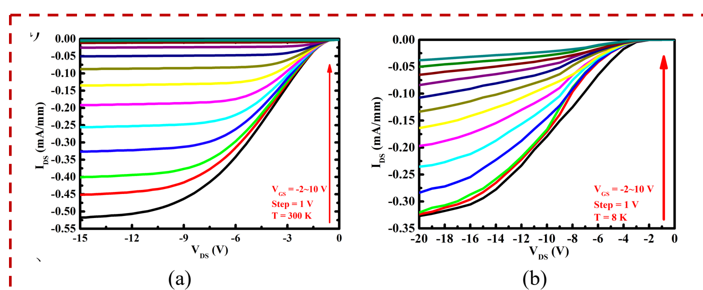
Fig.2. (a) Simulated band diagram, hole concentration and distribution of the designed InGaN/GaN and (b) Hole concentration profile from C-V measurement.

It was simulated that the peak hole density at the InGaN/GaN heterojunction was over 5.5 Å~ 10^{19} cm^{-3} with FWHM value of about 2 nm, indicating the formation of the 2DHG conducting channel with a high density (Fig. 2(a)). The carrier profile extracted from C-V indicates a hole accumulated at 95 nm from the surface, which is around the InGaN/GaN heterointerface (Fig. 2(b)).

2) <u>Achieve the first InGaN/GaN p-channel MOSFETs working at the cryogenic temperatures</u>

The Schottky and MOSFET were fabricated by using the standard semiconductor device process technique. The device was firstly isolated by the chlorine-based inductively coupled plasma dry etching. Then, Ni/Au (20/30 nm) stacks were deposited by electron-beam (EB) evaporation, followed by annealing at 500° C for 10 min in air ambient to form ohmic contacts. For the Schottky-type devices, Ti/Au (40/110 nm) bilayers were deposited by EB evaporation as the gate metal stacks. For MOSFET, a 60-nm Al_2O_3 was deposited by atomic layer deposition as the gate dielectric.

The fabricated InGaN/GaN heterojunction MOSFET shows an obvious 2DHG behavior. The DC output characteristics of the MOSFET at 300 K are displayed in Fig. 3(a). The depletion-mode (D-mode) behavior with an absolute source-drain current density, /I_{DS}/, 0.51 mA/mm for a negative gate voltage of − 2 V is observed, which is over 40 times higher than that reported in InGaN/GaN p-channel HFETs.[2] An ON/OFF ratio close to two orders of magnitude is obtained for this D-mode transistor. The threshold voltage V_{TH} of the MOSFET was estimated by extrapolating the linear region down the voltage axis to be about 10 V. The maximum transconductance gm is about 0.07 mS/mm at the drain bias V_{DS} of − 15 V. Further improvement can be obtained by reducing the parasitic resistances, such as reducing the ohmic contact resistance, or the gate-channel separation and the device dimensions. This significant p-channel behavior can be still observed in our developed InGaN-based MOSFET (Fig. 3 (b)) measured as



(a) (b)

Fig.3 (a) DC output and (b) semi-log plot of the transfer characteristics and the transconductance of the MOSFETs at 300 K.

low as 8 K.[3] Therefore, it can be verified that the p-channel characteristic is originated from not the acceptor doping but the polarization- induced 2DHG at the lower interface of InGaN/GaN heterojunction.

3) MOCVD growth of InGaN/GaN heterostructure on AlGaN/GaN template

The InGaN/GaN heterostructures were deposited on the AlGaN/GaN-on-Si HEMT templates by using the MOCVD. As a result of the large mismatch between InGaN and AlGaN, the strain and In composition should be different from that grown on sapphire substrate. The peak of the (002)-plane diffraction for the InGaN epilayer on the GaN/sapphire template is located at 33.93°, while this peak shifts to 33.98° when the InGaN is grown on the HEMT template. The out-of-plane lattice constant *c* of the GaN channel in the HEMT structure is smaller (5.179 Å) than that on the sapphire substrate (5.186 Å), which indicates a tensile strain inside the in-plane direction. The large strain in the GaN channel results in the different strain behaviors in the following InGaN layer.

The crystalline quality and the interface quality of the InGaN on HEMT templates can be improved by optimizing the growth conditions. The reflection fringes start to appear, indicating an abrupt interface morphology. The FWHM value is reduced to be 1260 arcsec. The In composition in the InGaN grown at 780°C on the HEMT template is ~14%, slightly lower than that grown at 760°C. Compared to the luminescence of the InGaN/GaN on HEMT at 760 °C, the intensity of the InGaN/GaN at 780 °C is increased. The *p*-type conductivity in the InGaN/GaN heterojunctions are further confirmed by the Hall effect and Seebeck measurements.[4]

4) Investigation on the interface states/defects at the MOS structure

The quality of the MOS interfaces for both n-channel and p-channel FETs strongly affects the electrical properties of the devices. The high-density interface states and traps could induce the unstable of the threshold voltage and increase the on-resistance. To ultimately improve the performance of GaN-based MOSFETs and realize real applications, a high-quality and stable MIS/MOS interface with low-density trap states both at and close to the interface is required. Figures 4 shows the energy band diagram of the interface traps at the n-GaN and p-GaN MOS structures. The first trap is interface state (Q_{it}), which is usually attributed to the dangling bonds or interface defects at the dielectric/semiconductor. The second one is oxide-related trap, one of which is called 'border traps' locating in the native GaO_x or the re-oxidation layer at MOS interface, while the other one is 'bulk traps' inside the dielectric layer. The positive fixed charges (Q_f) was also observed at MOS interface of the transition region between dielectric layer and semiconductor.

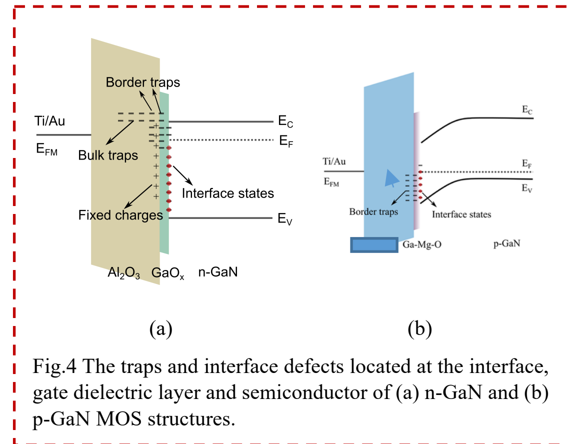


Fig.4 The traps and interface defects located at the interface, gate dielectric layer and semiconductor of (a) n-GaN and (b) p-GaN MOS structures.

We developed a two-step treatment remove the native oxides and contaminations. The procedure is $HF:H_2O$ (1:5) for 3 min at RT, followed by ammonium sulfide ($(NH_4)_2S:H_2O$ (1:5)) solution for 30 min at 70 °C. From TEM observation, the interfacial layer with Ga-O and Al-O oxides can be removed by the two-step treatment. The effective removal of the interface discontinuous layer greatly improves the electrical properties of the GaN MOS capacitors. The high frequency *C-V* curves exhibit deep depletion feature without inversion characteristics, due to the extremely low generation rate of the minority carriers. The MOS capacitor fabricated on the as-grown GaN exhibits a D_{it} value in the range of 10^{12} $cm^{-2}eV^{-1}$ of the effective energy level, which is normal for the GaN MOS interface on GaN

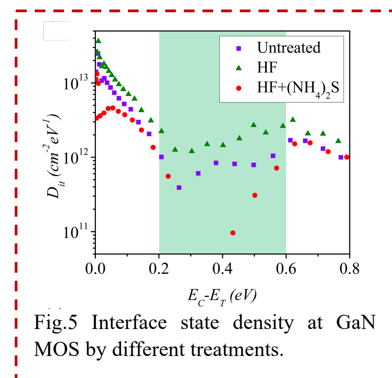


Fig.5 Interface state density at GaN MOS by different treatments.

substrate. By using HF etching, a slight increase in D_{it} is observed (Fig. 5), which may be due to the generation of nitrogen vacancy (N_v) or Ga dangling bonds on the fresh GaN surface after removing native GaO_x. The nitrogen-related vacancies and dangling bonds can be effectively saturated by the formation of Ga-S bonds through the surface modification process with $(NH_4)_2S$ passivation at high temperature, after which a drastic decrease of D_{it} (~10^{11} $cm^{-2}eV^{-1}$) is obtained. This value is approaching to the detection limit of the Terman method. These results indicate that the introduction of the $(NH_4)_2S$ passivation can effectively protect the GaN surface from the immediate re-oxidation during the following ALD process.

For the p-GaN MOS structure with ALD Al_2O_3 gate dielectric layer, it is found that due to the positive surface charges trapped in the Mg-Ga-O disordered region as a result of Mg segregation to the *p*-GaN surface, a large-density surface states on the order of 10^{13} cm^{-2} was observed. The high-density surface states lead to a large downward band bending of 1.2-1.6 eV.[5] Serious electrical hysteresis in both *I-V* and *C-V* characteristic was observed as a result of these high-density traps, bringing about the threshold voltage instability. To avoid the interfacial oxidized layer, we firstly propose to utilize the oxygen-free gate dielectric material silicon nitride (SiN_x) or calcium fluoride (CaF_2) for the *p*-GaN MIS capacitors together with the two-step surface treatment, and the interface trap states are greatly suppressed.

We compared the trapped charge densities at the *p*-GaN MO(I)S interfaces with different gate dielectric layers after the same chemical treatment, as shown in Table I. As can be seen, the trapped charge density at the SiN_x/*p*-GaN MIS interface is at least 1-2 orders of magnitude lower than the Al_2O_3, SiO_2, or CaF_2/*p*-GaN MO(I)S structures. In addition, the frequency dispersion is also suppressed by using SiN_x dielectric layer, which is another advantage over CaF_2 insulator.[6] The sputtered SiN_x dielectric can be more suitable for the real applications, due to its amorphous feature, high thermal conductivity and good environmental stability.

Table 1. Summarized trapped charge density at the *p*-GaN MO(I)S interfaces with different gate dielectric layers

	ALD-Al_2O_3	SiO_2	CaF_2	SiN_x
Trapped charge density (cm^{-2})	1.3×10^{13}	4.2×10^{12}	5.6×10^{11}	5.5×10^{10}

5) Fabrication of the GaN-based complementary power circuits

The device was firstly isolated by the chlorine-based inductively coupled plasma dry etching. Then, the AlGaN/GaN HEMTs were fabricated using the standard device processing. For the p-channel FETs, the optimized MIS structure was fabricated. A relatively thick SiN_x of 60 nm was deposited by sputtering as the gate dielectric, followed by the Ti/Au (40/110 nm) bilayers as the gate metal stacks. Finally, the integrated circuits were designed and connected. The AlGaN/GaN heterostructure and InGaN/GaN heterostructure showed the n-channel and p-channel properties, respectively. The maximum drain current density was achieved to be ~ 350 mA/mm. To reduce the leakage current of the HEMTs, the surface treatment using slightly plasma etching with Ar gas was utilized to remove the native oxides. The ON/OFF ratio as high as 10^{10} was achieved, indicating a high performance.

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５．主な発表論文等

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掲載論文のDOI（デジタルオブジェクト識別子） https://doi.org/10.1063/1.5010952	査読の有無 有
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３．雑誌名 Optics Express	６．最初と最後の頁 8935～8935
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1．著者名 Wu Haihua、Sang Liwen、Li Yumeng、Teraji Tokuyuki、Li Tiefu、Imura Masataka、You Jianqiang、Koide Yasuo、Toda Masaya、Liao Meiyong	4．巻 2
2．論文標題 Reducing intrinsic energy dissipation in diamond-on-diamond mechanical resonators toward one million quality factor	5．発行年 2018年
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1．著者名 Matsuura Haruka、Onuma Takeyoshi、Sumiya Masatomo、Yamaguchi Tomohiro、Ren Bing、Liao Meiyong、Honda Tohru、Sang Liwen	4．巻 9
2．論文標題 MOCVD Growth and Investigation of InGaN/GaN Heterostructure Grown on AlGaN/GaN-on-Si Template	5．発行年 2019年
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４．発表年 2018年

〔図書〕　計0件

〔産業財産権〕

〔その他〕

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６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考