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科学研究費助成事業　　研究成果報告書

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研究課題名（和文）高エネルギー効率演算を可能とする超伝導シナジー集積回路システムの研究

研究課題名（英文）Synergistic Integration of Novel Superconductor Electronics for Energy-Efficient Computing Accelerators

研究代表者

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研究成果の概要（和文）：世界初の超伝導断熱 SHA-3 ブロック置換ユニット チップを開発しました。このチップには 13,000 個を超える超伝導ジョセフソン接合デバイスが含まれており、約 18.2 aJ/op のエネルギー消費で最大 7 GHz で動作します。より大規模なチップのテストが進行中です。その後、私たちは、AQFP と RSFQ (高速単一磁束量子) の 2 つの超伝導技術を組み合わせた新しいアーキテクチャを提案しました。これは、トランスポート トリガー アーキテクチャ (TTA) と呼ばれ、ポスト量子暗号ベンチマークで計算パフォーマンスとエネルギー効率の両方で有望です。

研究成果の学術的意義や社会的意義
We show that hashing operations are possible in superconductor technology and that there is viable path towards using multiple superconductor logics intelligently in this space. This helps improve cybersecurity for society while reducing power consumption to support ICT.

研究成果の概要（英文）：The application space for cryptography is an excellent target for superconductor electronics because it has intensive computational needs and high-power workloads. We developed the world's first superconducting adiabatic SHA-3 block permutation unit chip to showcase the basic cryptographic hashing operations using adiabatic quantum-flux-parametron (AQFP) technology. It is a scaled down version of SHA-3 containing over 13,000 superconductor Josephson junction devices and operated up to 7 GHz with an energy dissipation of about 18.2 aJ/op. A larger scale chip is undergoing testing. Inspired by these results, we proposed a new architecture that combines two superconductor technologies: AQFP and RSFQ (rapid single flux quantum) technologies. It is a transport triggered architecture (TTA) that shows promise in both computational performance and energy efficiency in post-quantum cryptography benchmarks. This synergistic architecture will serve as the basis for future projects.

研究分野：Superconductor electronics, adiabatic computing

キーワード：superconductor　adiabatic　EDA　Josephson junction　AQFP　RSFQ　cryptography　hash

１．研究開始当初の背景

Driven by trends in cloud computing, big data, and the Internet of Things (IoT), there is an increasing demand for data processing, storage, and transmission. This can be observed by the growing market size for data centers with trends indicating over $600 billion USD in growth by 2026 [1]. Studies also suggest that the electricity demand to support information and communications technology (ICT) will surpass 20% of the total electricity usage by 2030 [1]. The power to continuously perform computationally expensive tasks such as cryptographic proof-of-work for blockchains is surpassing 140 TWh/year [2]. To combat these trends, one possibility is to consider alternative computing technologies.

Superconductor digital electronics may pave an avenue towards ultra energy-efficient computing. Notably, the adiabatic quantum-flux-parametron (AQFP) based on a pair of superconductor Josephson junction (JJ) devices has been demonstrated to dissipate as little as 1.4 zJ per device [4] while still operating at GHz clock frequencies. Fig. 1a shows the basic schematic of the AQFP while illustrating its basic operation. Further, Fig. 1b shows how multiple AQFPs can be combined to create majority-based logic gates. In previous work, the very first superconductor adiabatic microprocessor called MANA was built using AQFPs [3]. While it was a significant demonstration, it also revealed challenges such as low integration density, especially in memory-like circuits such as the register file of the MANA microprocessor. It also showed how difficult it was to close the numerous data feedback loops that the microprocessor had while still operating at high clock rates. One approach is to further develop the AQFP technology and design methodologies to overcome these challenges. Another approach is to investigate combining AQFP technology with other superconductor electronics such as RSFQ logic in which their synergistic usage could greatly enhance a system's performance. Lastly, another method is to investigate new architectures and/or specific workloads that are still impactful but greatly showcase the strengths of AQFP and/or superconductor electronics. In this work, we propose the above as a step towards building next-generation performance-rich energy-efficient computing platforms using superconductor electronics.

２．研究の目的

The objective of this research is to identify meaningful, impactful workloads that superconductor electronics can tackle and then design a circuit that specifically targets that workload. In this circuit design, we will consider opportunities to combine and integrate different superconductor logic families such as AQFP and RSFQ technologies. The combination of multiple technologies should be done in a synergistic manner such that the strengths of the corresponding technologies are showcased, further enhancing the overall performance in handling the target workload. Ultimately, this work addresses the need for new computing approaches to handle the high electricity demand to support information and communications technologies (ICT). With significantly lower power consumption to support ICT with superconductor electronics, society can benefit in a more enhanced form of ICT that has lower negative impact on the environment we live in today.

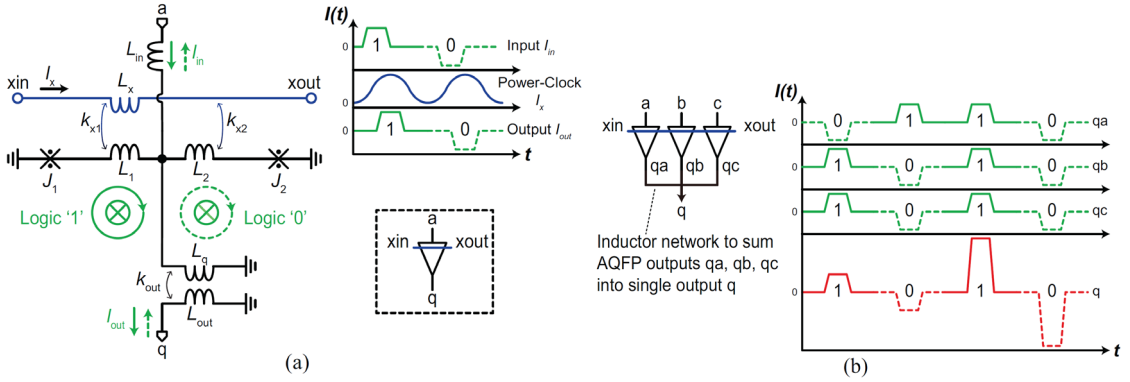

Fig. 1: Basic operation of the AQFP. (a) The schematic of the AQFP with a corresponding illustration of how data is represented in terms of positive (logic '1') and negative current (logic '0') along with a typical logic symbol. (b) Logic gates are built by combining multiple AQFPs through an inductor network where the output currents of each AQFP are summed up creating natural majority logic gates.

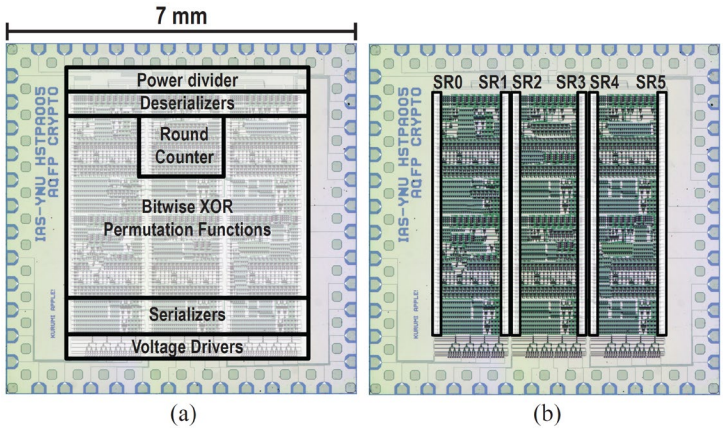

Fig. 2: AQFP SHA-3 block permutation unit chip. (a) Main components of the chip. (b) Debug shift registers (SRs) for each clocked column.

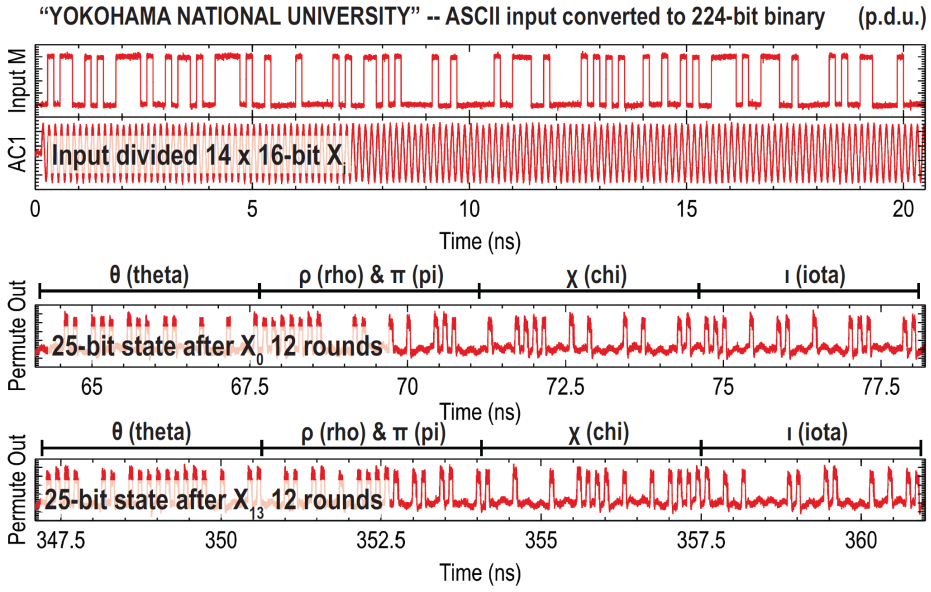

Fig. 3: Serialized experimental input and output waveforms operating at 7 GHz in 4.2 K liquid He. The output waveforms are the intermediate permutation results as X_0 is absorbed and later as X_{13} is absorbed.

３．研究の方法

The approach for this research project was implemented through 4 driving tasks:

Task 1 (T1): Project discovery
In this task, we will prepare a design, simulation, and analysis environment to support novel superconductor devices. We will ramp up our fundamental knowledge on SFQ, AQFP, and cryotrons. A new compute server will be purchased to perform research tasks.

Task 2 (T2): Superconductor technology analysis
We will investigate each technology and identify their strengths and weaknesses. We will also try to find new operation modes and/or use unexploited phenomena. This includes performing analog simulation using Python scripts and freely available superconductor circuit simulations such as JoSIM.

Task 3 (T3): Architecture analysis
We will conduct design studies on architecture candidates and may also develop completely new architectures considering the results from task 2. This includes modeling some architectures using a hardware description language (HDL) such as Verilog or VHDL and running high-level simulations in tools such as Siemens ModelSim.

Task 4 (T4): Prototype accelerator development
This period will focus on the design, implementation, and demonstration of a chosen accelerator at a small prototype scale. The design will be done in industry-leading integrated circuit (IC) design tools such as Cadence Virtuoso available through the VDEC program in Japan. We will also comprehensively outline the technical needs for future VLSI scaling.

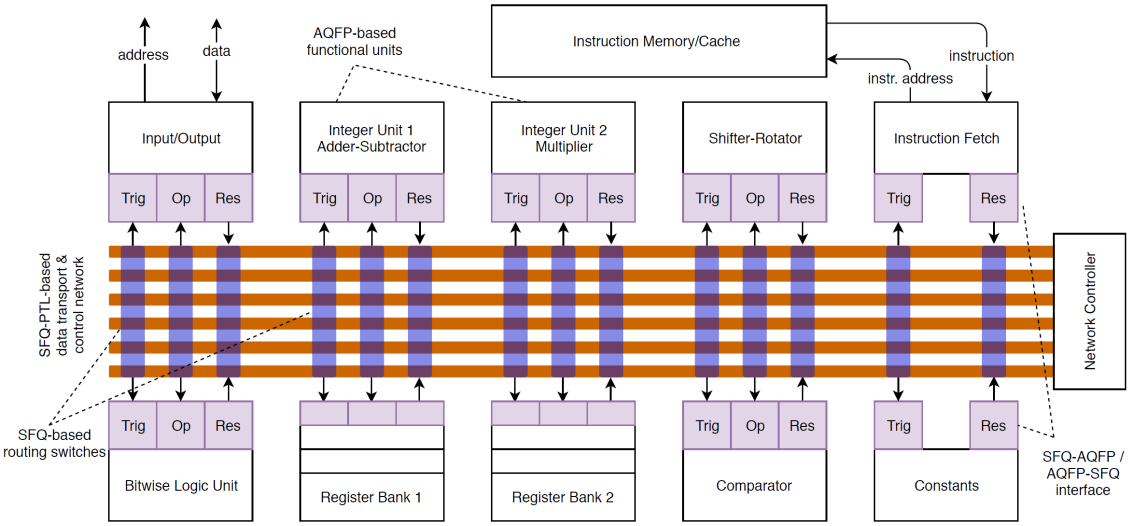

Fig. 4: Conceptual diagram of a hybrid AQFP/RSFQ-based transport triggered architecture (TTA) processor. Functional units such as adders/subtractors/bitwise logic units are implemented in energy-efficient AQFP logic. The data transport and control network are implemented using RSFQ and PTLs. Between the data transport and the functional units are RSFQ-AQFP and AQFP-RSFQ interfaces.

4．研究成果

Our investigation determined that the application space of cryptography might be worth pursuing for superconductor electronics. One of the most intensive, power consumption heavy forms of computation is the “proof-of-work” operation in the block validation of Bitcoin. The proof-of-work alone uses over 140 TWh/year [2]. The proof-of-work requires performing numerous hashing operations from the SHA-2 algorithm. We looked at the operations for the next generation hashing algorithm known as SHA-3 and realized it was a very good fit for superconductor electronics because (1) data feedback is regularly and simple to design, (2) the control circuit is a straightforward counter, and (3) there is usually no need for centralized memory (like the very large footprint register file in the MANA demo) to perform the hashing algorithm. We developed a demo chip that implements a scaled down version of SHA-3’s block permutation unit which carries out the hashing state transformations. The chip comprises over 13,000 JJs on a 7 mm x 7 mm die as shown in Fig. 2. It successfully operated in liquid He up to 7 GHz with an estimated energy dissipation of 18.2 aJ/op. Output waveforms showing the intermediate results of the permutation unit are shown in Fig. 3. This is the largest AQFP chip ever demonstrated at GHz clock frequencies and shows that AQFP technology is very capable of performing hashing operations popular for cybersecurity.

Next, we proposed a transport triggered architecture (TTA) based on a synergistic blend of AQFP and RSFQ technologies. TTA recently caught attention because of its superior performance in post-quantum cryptography benchmarks versus RISC-V implementations [4]. Fig. 4 illustrates our proposal where several small functional units that carry out computation operations are implemented in AQFP to leverage their parallel-friendly clock network and extremely low power dissipation. These functional units are all connected to a high-speed serialized transport network implemented in RSFQ technology to leverage ballistic passive transmission line signal delivery and ultra-high-speed clock rates suitable for fast serialization/deserialization of data. This architecture will serve the basis for follow-on projects in the future towards low power dissipation cybersecurity acceleration as we become a more information-centric society where data privacy and security are becoming more and more important.

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２．論文標題 Low-Latency Adiabatic Quantum-Flux-Parametron Circuit Integrated With a Hybrid Serializer/Deserializer	５．発行年 2022年
３．雑誌名 IEEE Access	６．最初と最後の頁 133584～133590
掲載論文のDOI（デジタルオブジェクト識別子） 10.1109/ACCESS.2022.3230447	査読の有無 有
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１．著者名 Hironaka Yuki、Meher Sukanya S.、Ayala Christopher L.、He Yuxing、Tanaka Tomoyuki、Habib Mustapha、Sahu Anubhav、Inamdar Amol、Gupta Deepnarayan、Yoshikawa Nobuyuki	４．巻 33
２．論文標題 Demonstration of Interface Circuits for Adiabatic Quantum-Flux-Parametron Cell Library Using an Eight-Metal Layer Superconductor Process	５．発行年 2023年
３．雑誌名 IEEE Transactions on Applied Superconductivity	６．最初と最後の頁 1～5
掲載論文のDOI（デジタルオブジェクト識別子） 10.1109/TASC.2023.3244147	査読の有無 有
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掲載論文のDOI（デジタルオブジェクト識別子） 10.1109/TASC.2023.3258366	査読の有無 有
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A full-custom design flow and a top-down RTL-to-GDS flow for adiabatic quantum-flux-parametron logic using a commercial EDA design suite

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2024年

１．発表者名 Christopher L. Ayala, Nobuyuki Yoshikawa, Yu Hoshika, and Yuto Omori
２．発表標題 Multi-GHz Zeptojoule Computing Using Emerging Adiabatic Superconductor Circuits
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〔図書〕　計0件

〔産業財産権〕

〔その他〕

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６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考

７．科研費を使用して開催した国際研究集会

〔国際研究集会〕　計0件

８．本研究に関連して実施した国際共同研究の実施状況

共同研究相手国	相手方研究機関